

Round Rock 13.3" Schematics Document

Haswell ULT

2013-06-28
REV : SSI

DY : None Installed
XDP: For CPU XDP Debug Port installed
PCH_XDP: For PCH XDP Debug Port installed

<Core Design>



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Title

Cover Page

Size
A3

Document Number

Round Rock 13.3" UMA

Rev
X00

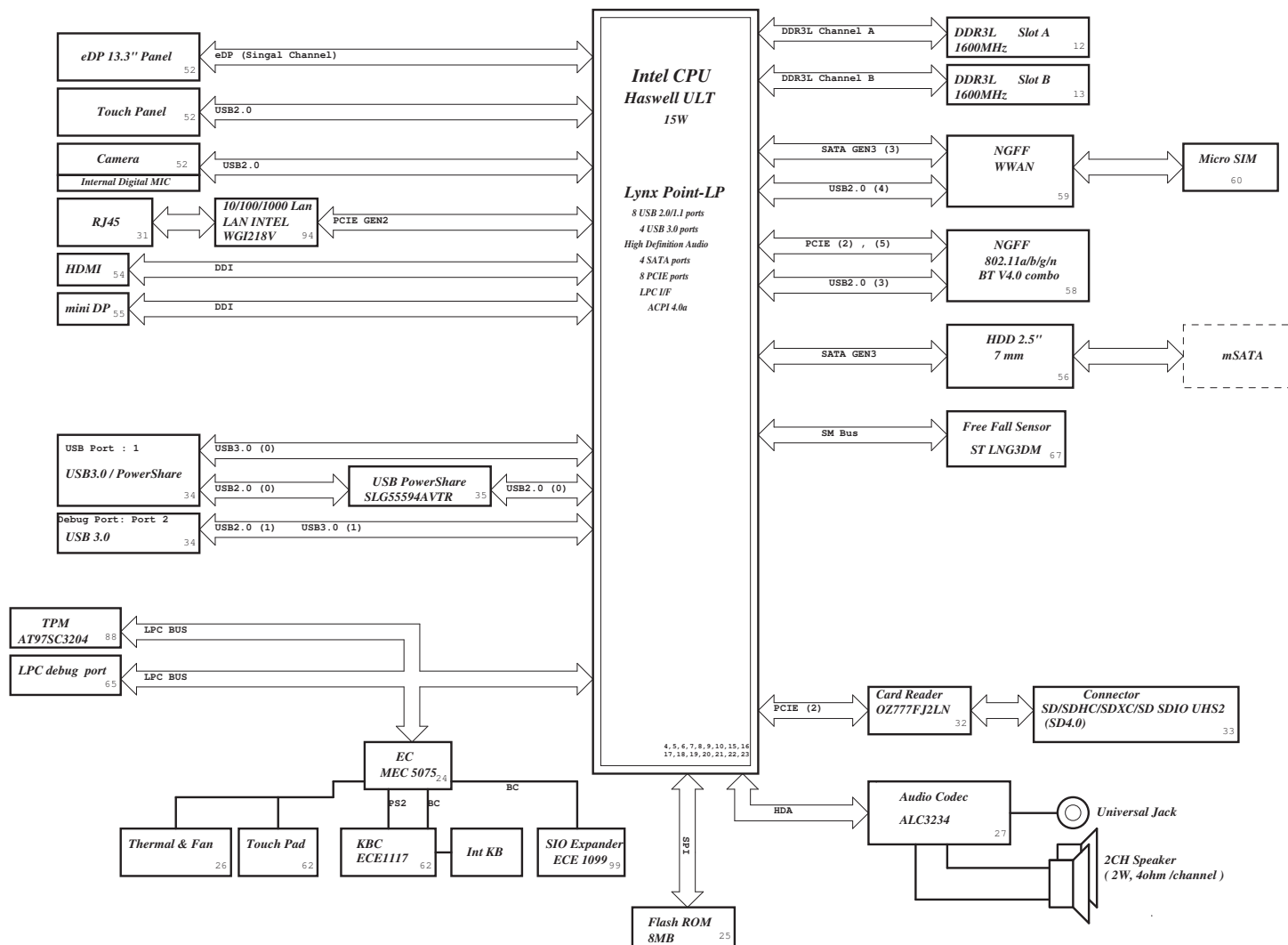
Date: Friday, June 28, 2013

Sheet 1 of 107

Round Rock 13.3" Block Diagram

Project code : 91.40A01.001
PCB P/N : 13229
Revision : X00

CHARGER BQ24715 44	
INPUTS	OUTPUTS
AD+ BT+	DCRATOUT
SYSTEM DC/DC TPS51275 45	
INPUTS	OUTPUTS
DCRATOUT	3.3V_AUX_S5 3.3V_S5 5V_S5
CPU DC/DC TPS51622 46-47	
INPUTS	OUTPUTS
DCRATOUT	VCC_CORE
SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCRATOUT	ID05V_M
SYSTEM DC/DC TPS51363 & APL5338 49	
INPUTS	OUTPUTS
DCRATOUT	ID05V_S3 ID0675V_S0 DDR_VREF_S3
Load Switches 36	
INPUTS	OUTPUTS
5V_S3 3.3V_S3	5V_S0 3.3V_S0 3.3V_SS_PCH 3.3V_M 3.3V_LAN ID05V_MODPHY ID05V_S0
PCB LAYER(FR4-6 Layer)	
L1:Top L2:PW/GND L3:Signal L4:Signal L5:PW/GND	L6:Bottom



5

4

3

2

1

D

C

B

A

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CPU (PCIE/DMI/FDI)

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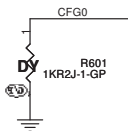
Rev
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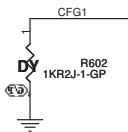
Sheet 3 of 107

SSID = CPU

EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	0: Lane Reversed 1: (Default) Normal Operation; No stall

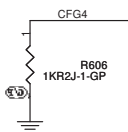


PCH/PCH LESS MODE SELECTION	
CFG1	0: Lane Reversed 1: (Default) Normal Operation

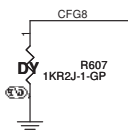


X01-20130204

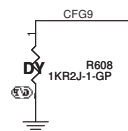
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



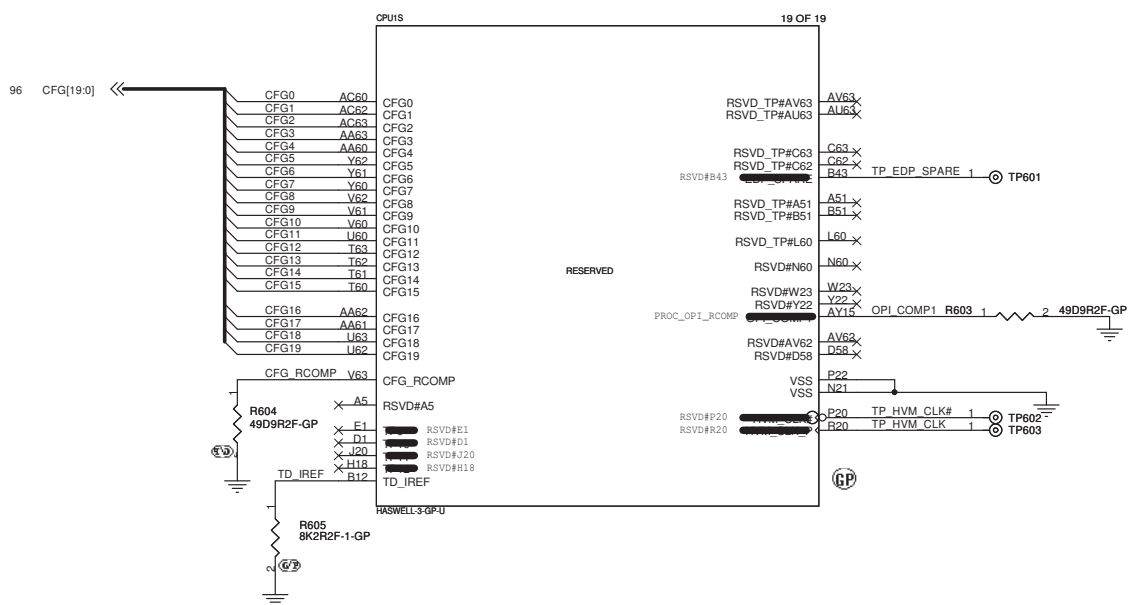
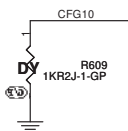
ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegrardless of the locking of the unit



NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0: No VR support SVID is present The chip will not generate (OR Respond to) SVID activity



SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED



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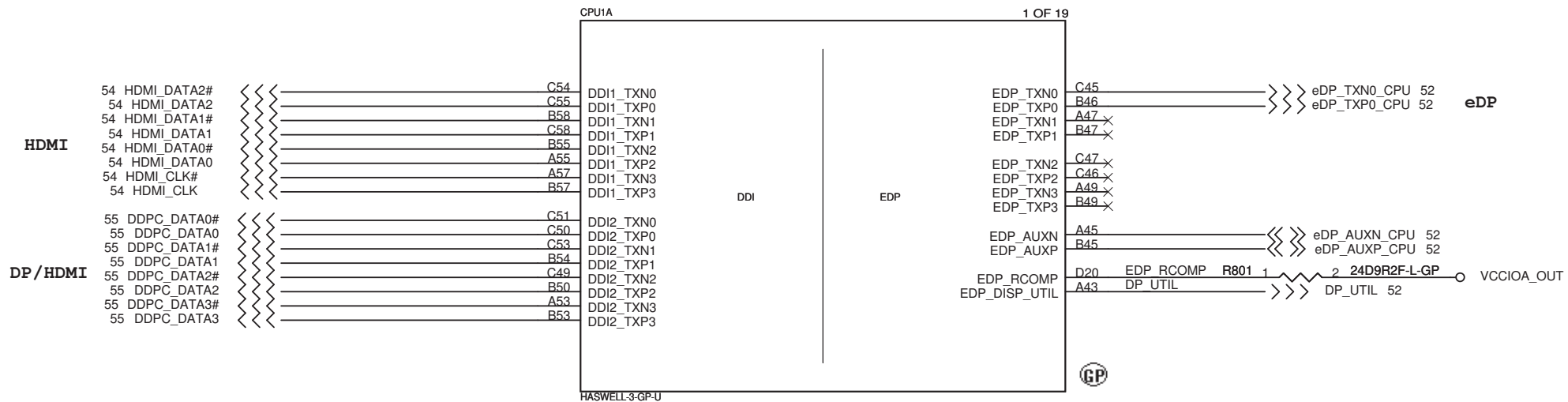
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Title: **CPU (RESERVED)**

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Date: Friday, June 28, 2013 Sheet: 6 of 107

SSID = CPU



DDI	HDMI	Display Port
DDI_TXN0	HDMI_DATA2_N	DP_LANE0_N
DDI_TXP0	HDMI_DATA2_P	DP_LANE0_P
DDI_TXN1	HDMI_DATA1_N	DP_LANE1_N
DDI_TXP1	HDMI_DATA1_P	DP_LANE1_P
DDI_TXN2	HDMI_DATA0_N	DP_LANE2_N
DDI_TXP2	HDMI_DATA0_P	DP_LANE2_P
DDI_TXN3	HDMI_CLK_N	DP_LANE3_N
DDI_TXP3	HDMI_CLK_P	DP_LANE3_P

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Title

CPU (DDI/EDP)

Size
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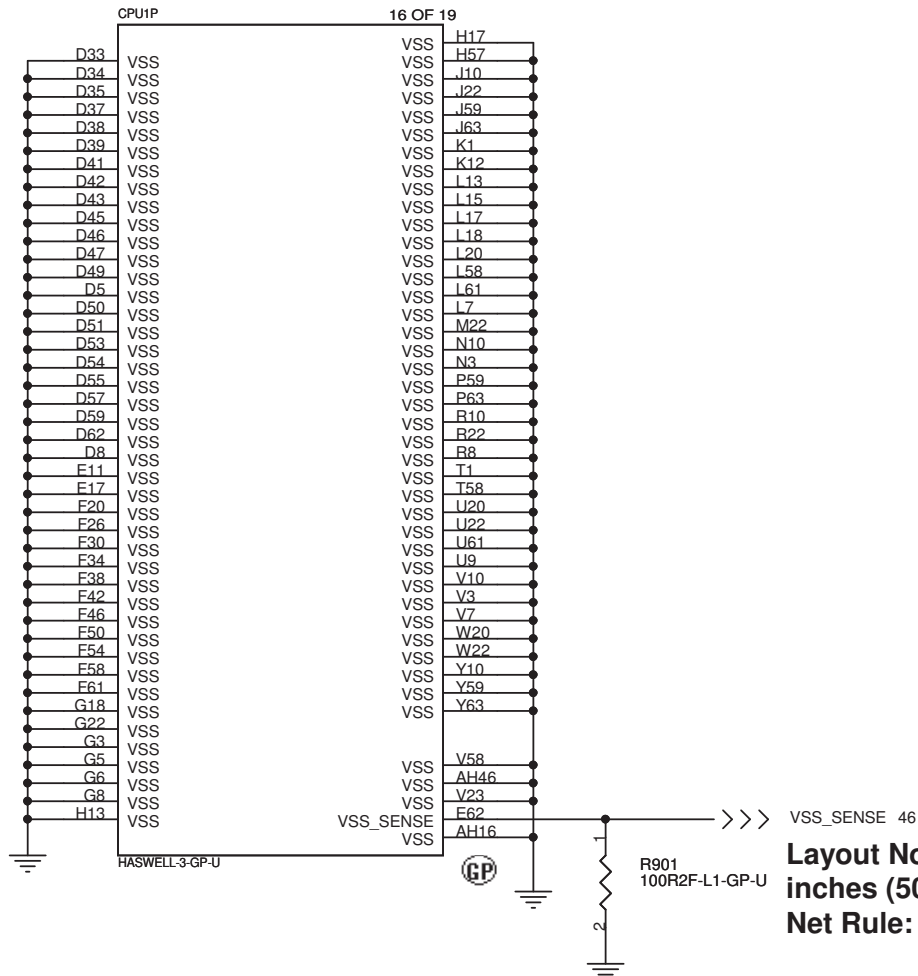
Round Rock 13.3" UMA

Rev
X00

Date: Friday, June 28, 2013

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SSID = CPU



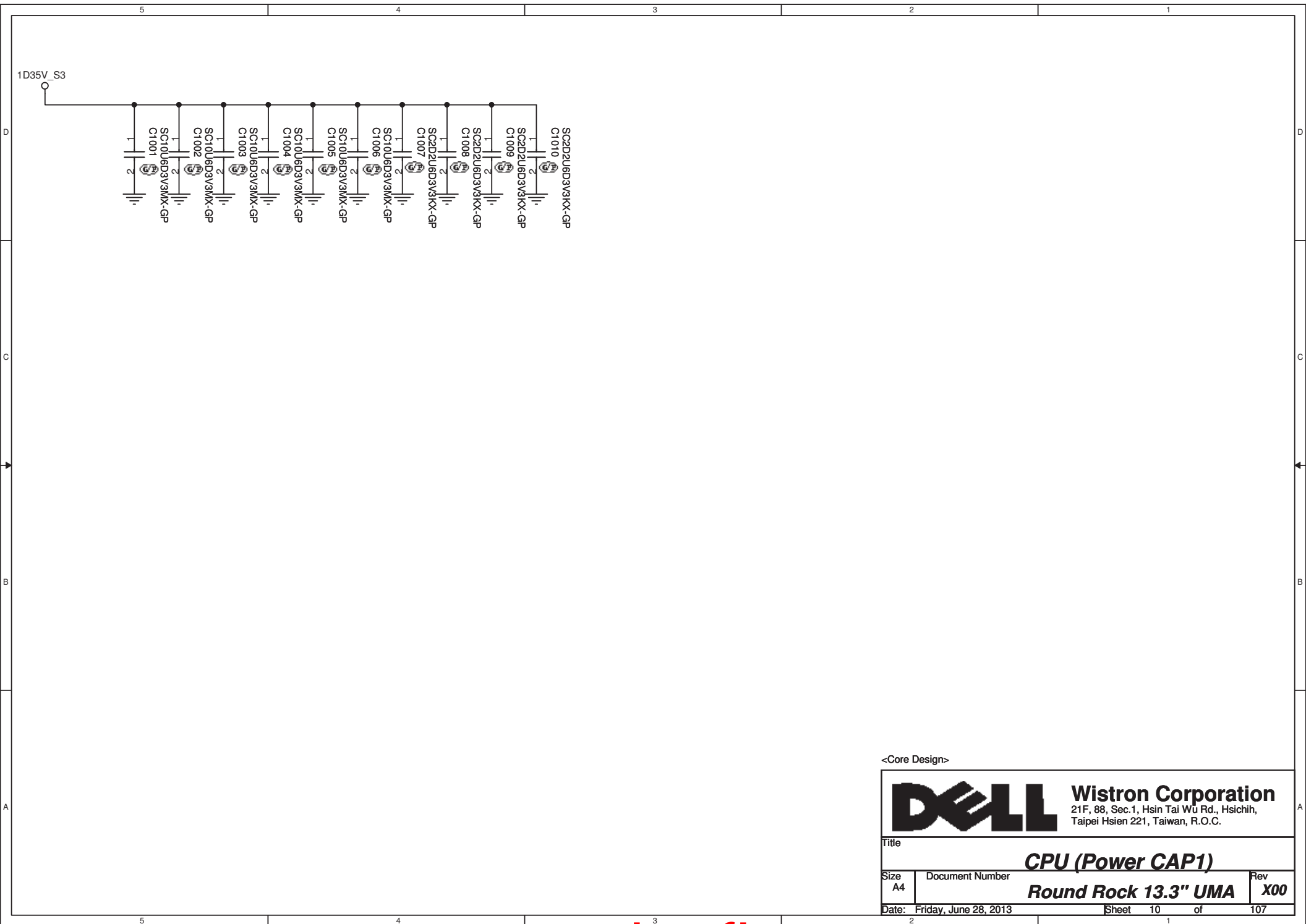
Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.
Net Rule: VCC_SENSE and VSS_SENSE differential signals

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Title			CPU (VSS)	
Size A4	Document Number		Round Rock 13.3" UMA	
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Title			
CPU (Power CAP1)			
Size A4	Document Number		Rev X00
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Title

CPU (Power CAP2)

Size
A

Document Number

Round Rock 13.3" UMA

Rev

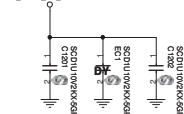
X00

Date: Friday, June 28, 2013

Sheet 11 of 107

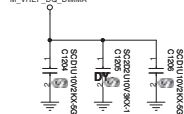
Layout Note:

M_VREF_CA_DIMMA



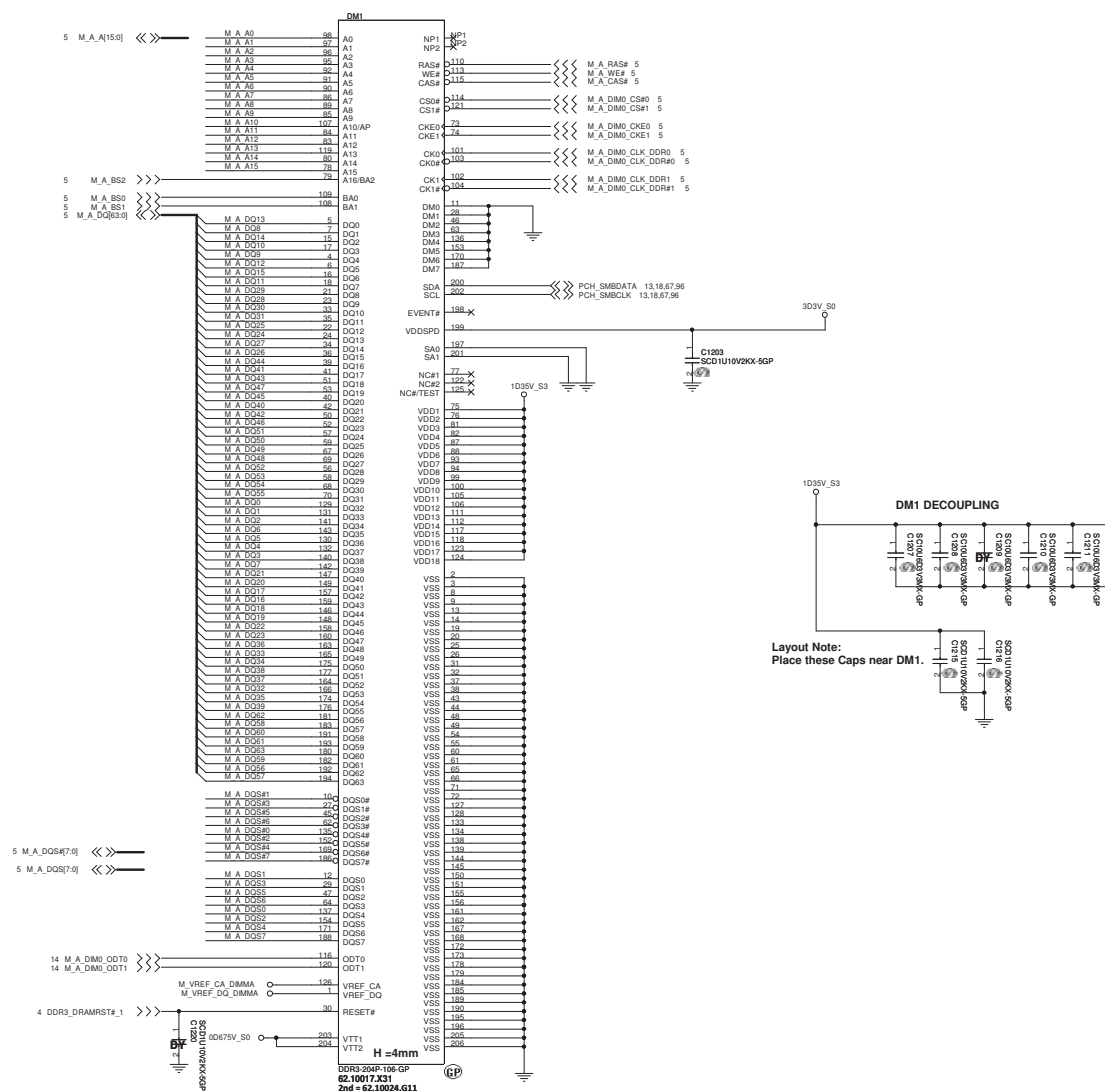
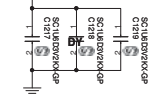
Layout Note:

M VREF DQ DIMMA



0D675V S0

Place these caps
close to VTT1 and VTT2.



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

Layout Note:
Place these Caps near DM1.

<Core Design>

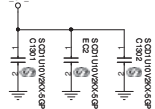


Title			
DDR3L-SODIMM1			
Size A2	Document Number		Rev X00
Round Rock 13.3" UMA			
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SSID = MEMORY

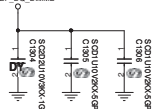
Layout Note:

Place these caps close to VREF_CA
M VREF CA DIMMB



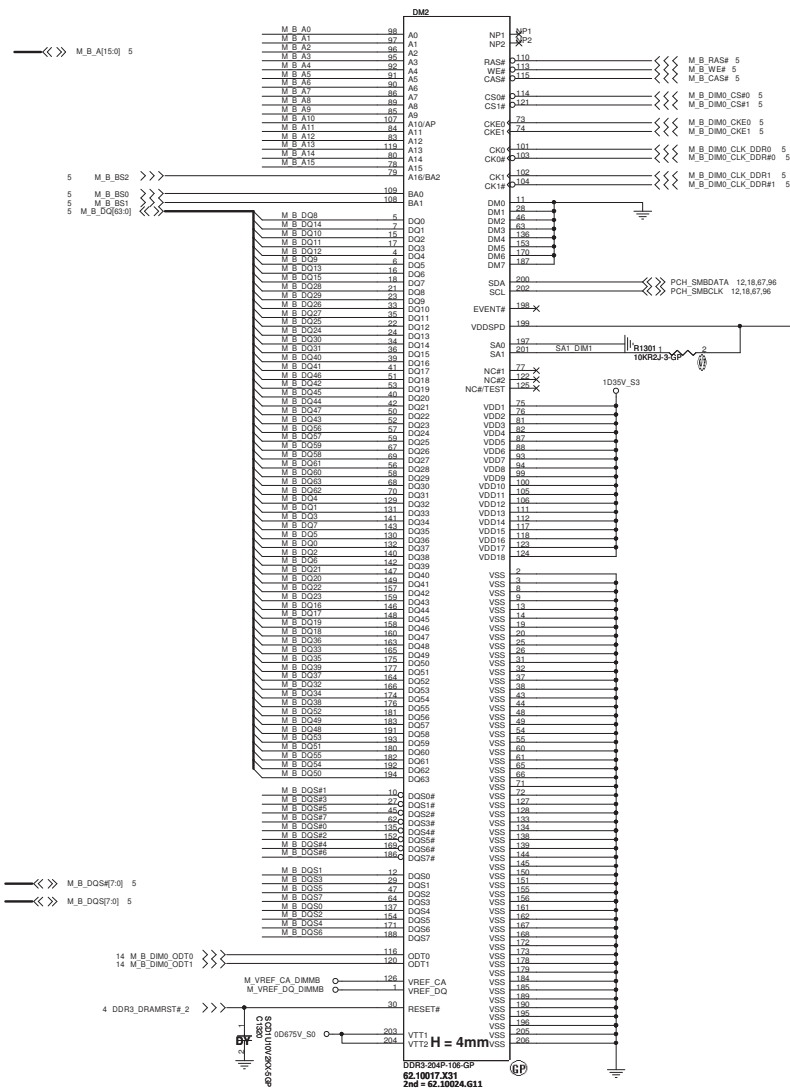
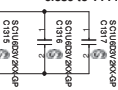
Layout Note:

Place these caps close to VREF_DQ



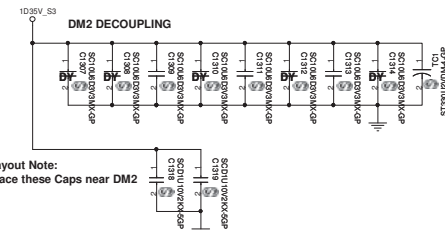
0D675V_S0

**Place these caps
close to VTT1 and VTT2**



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

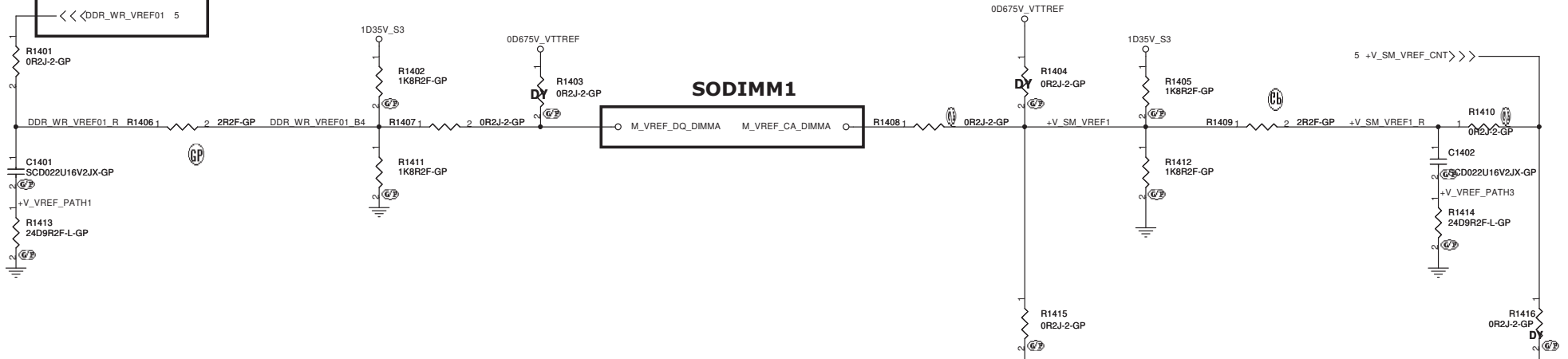
SO-DIMMB is placed farther from the Processor than SO-DIMMA



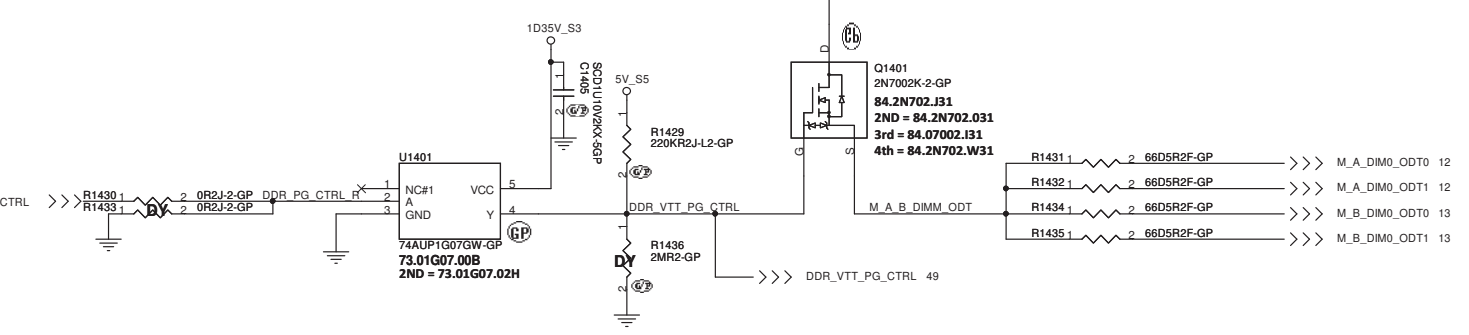
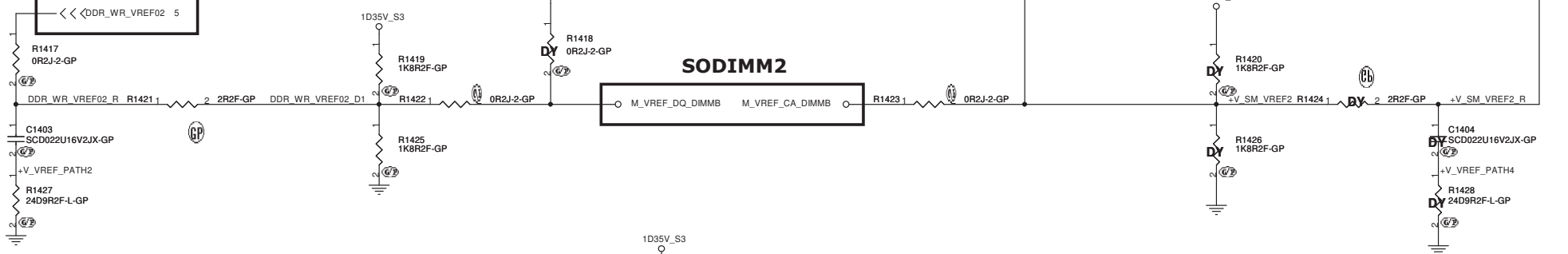
Layout Note:
Place these C

SSID = MEMORY VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation

SA_DIMM_VREFDQ
Driven by process (PIN#AR51)



SB_DIMM_VREFDQ
Driven by process (PIN#AP51)



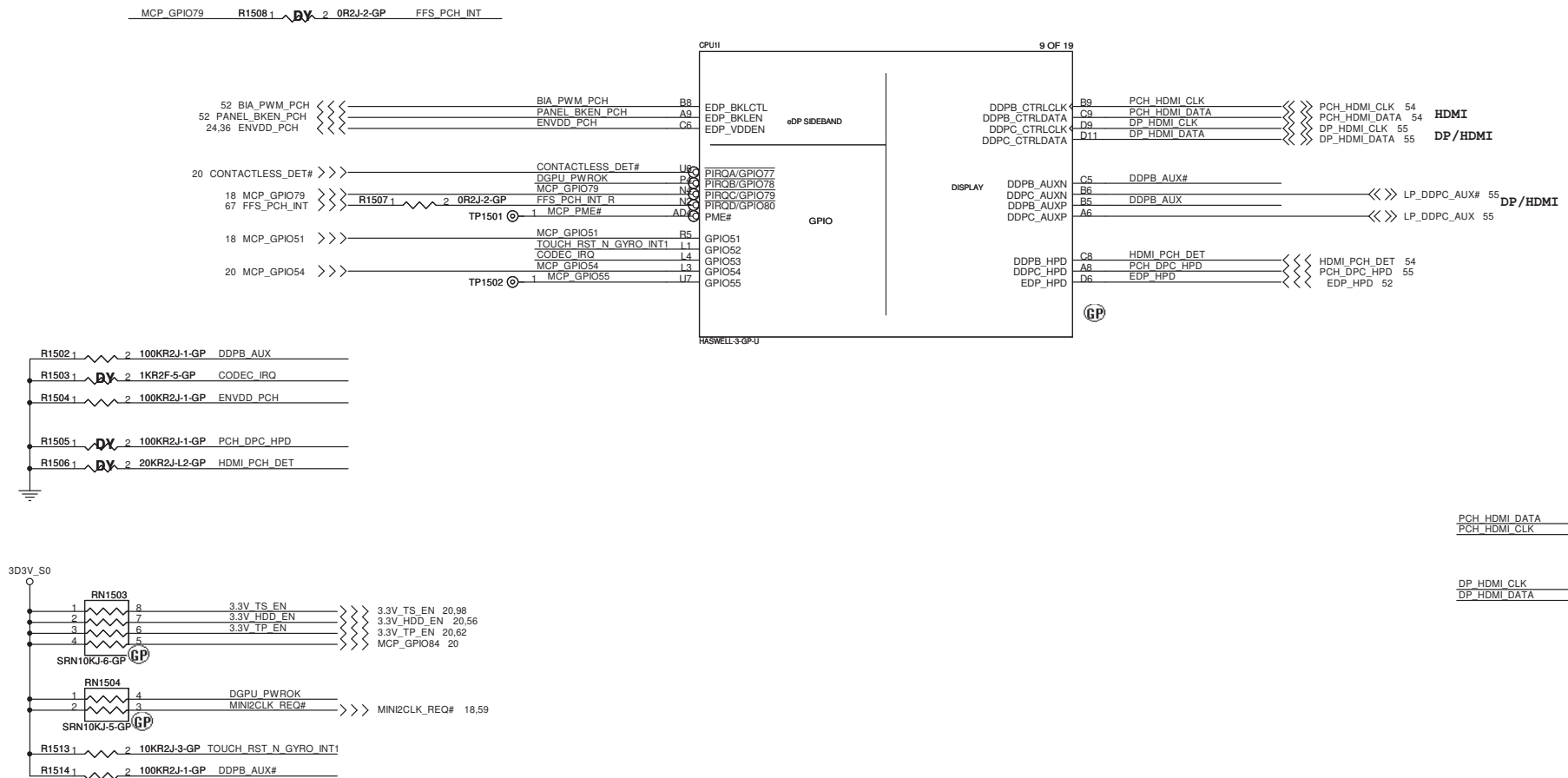
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Title: **M1 & M3 Implementation**

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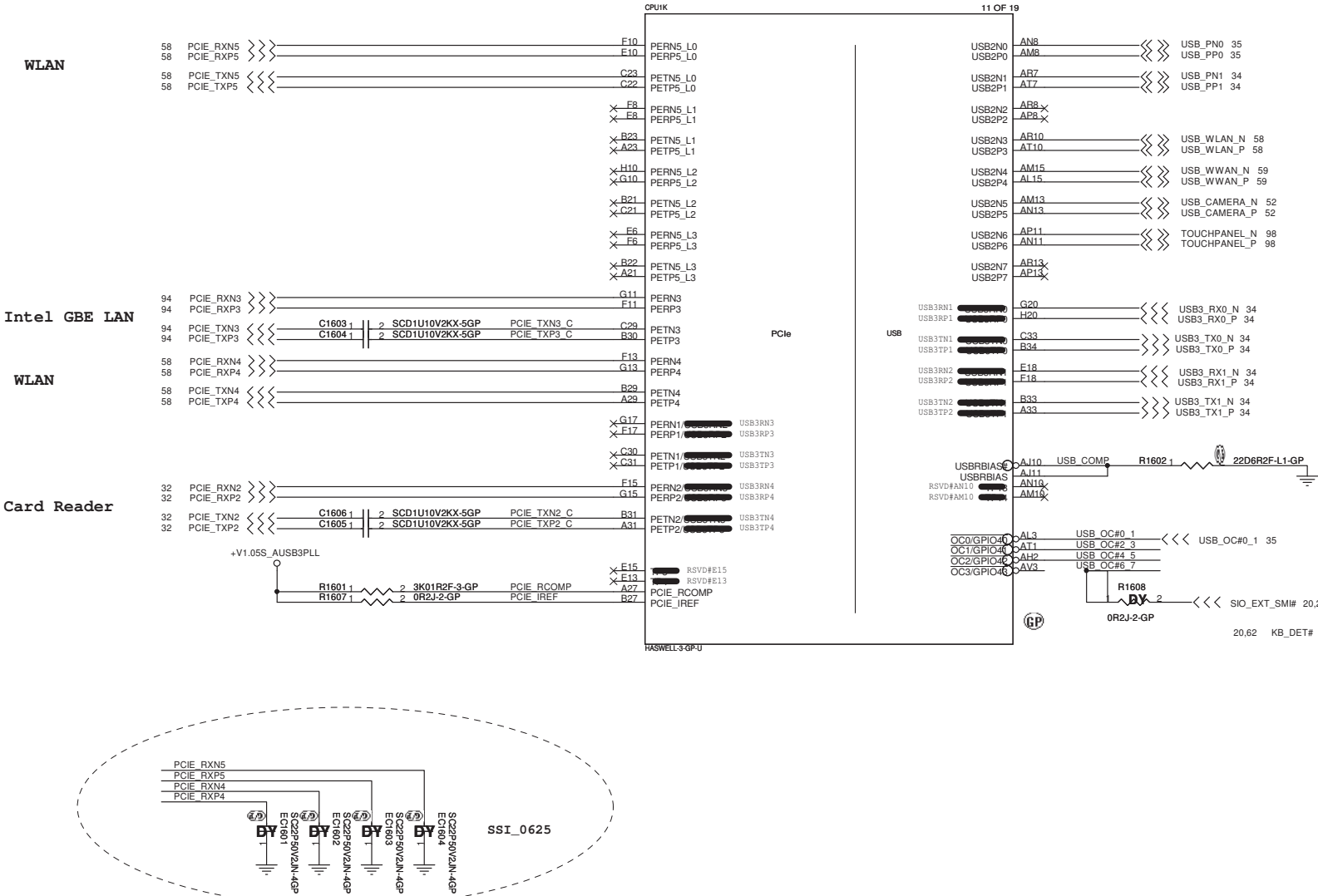
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Title CPU (DDI/PCI)		
Size A3	Document Number Round Rock 13.3" UMA	Rev X00
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SSID = PCH

USB2.0 Table	
Pair	Device
0	USB port 2 (usb charger)
1	USB port 1 (win debug)
2	N/A
3	WLAN (BT)
4	WWAN
5	CAMERA
6	Touch Panel
7	N/A

USB3.0 Table	
Pair	Device
1	USB port 1
2	USB port 2
3	N/A
4	N/A

Shark Bay ULT:
USB Ext. port 1
External debug port use on Shark Bay platform



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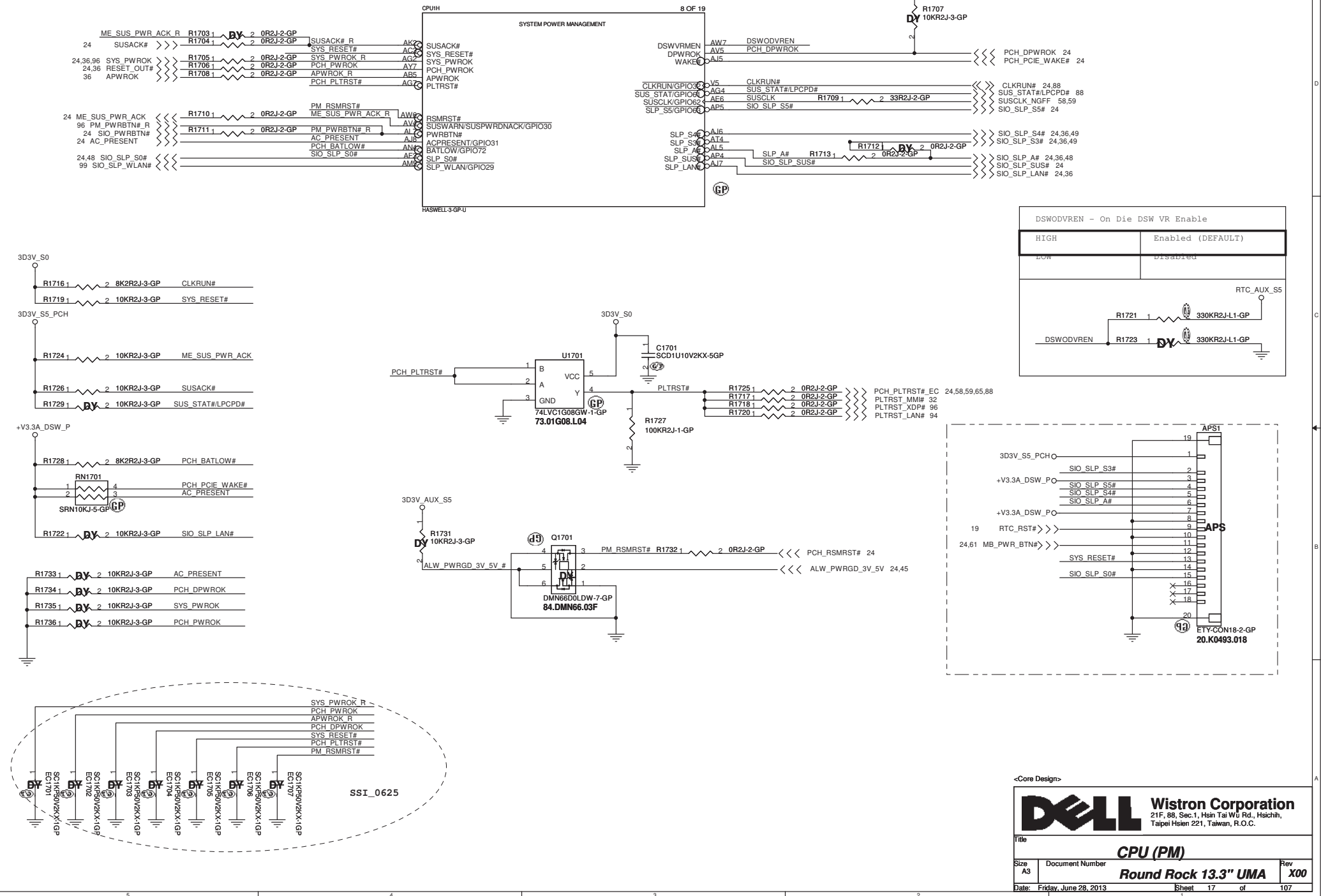
Title: **CPU (PCIE/USB)**

Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

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SSID = PCH

NOTE:
PWRBTN# Integrated Pull-Up.



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Title: **CPU (PM)**

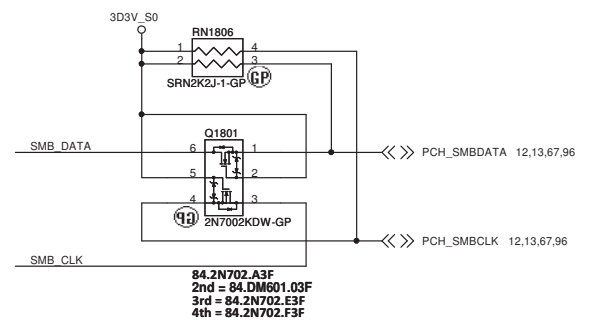
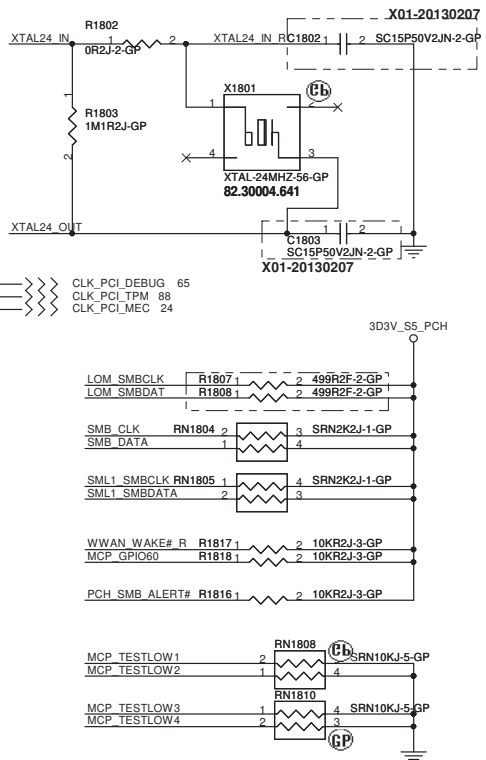
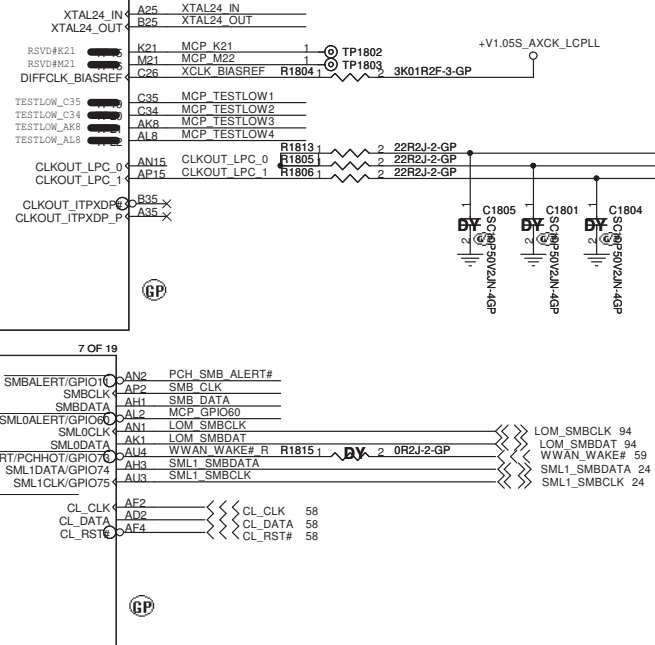
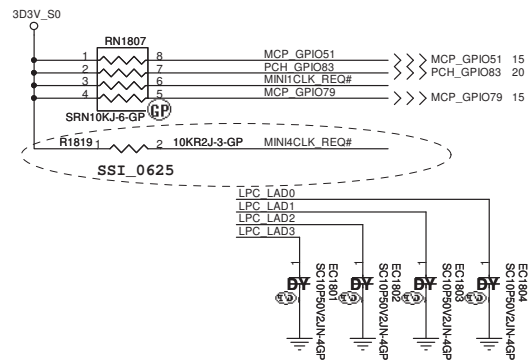
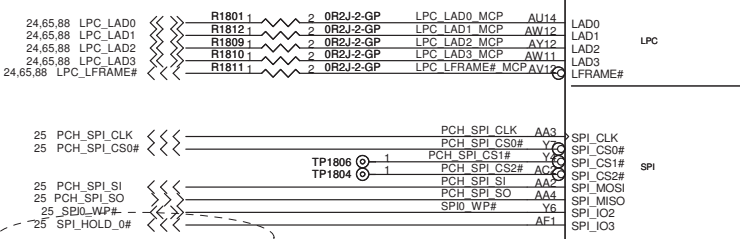
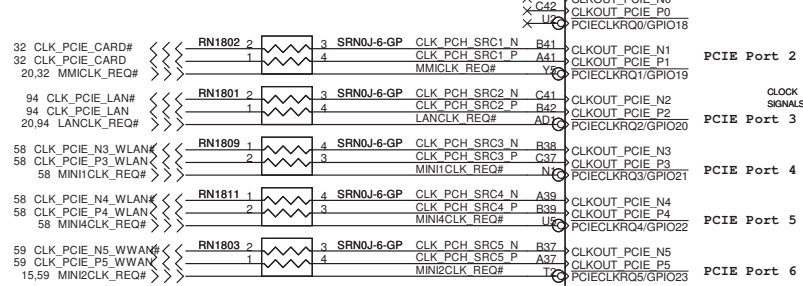
Size: A3 Document Number: **Round Rock 13.3" UMA** Rev: **X00**

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SSID = PCH

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

PCIECLKRQn# is route to PCIE Port (n+1)



<Core Design>

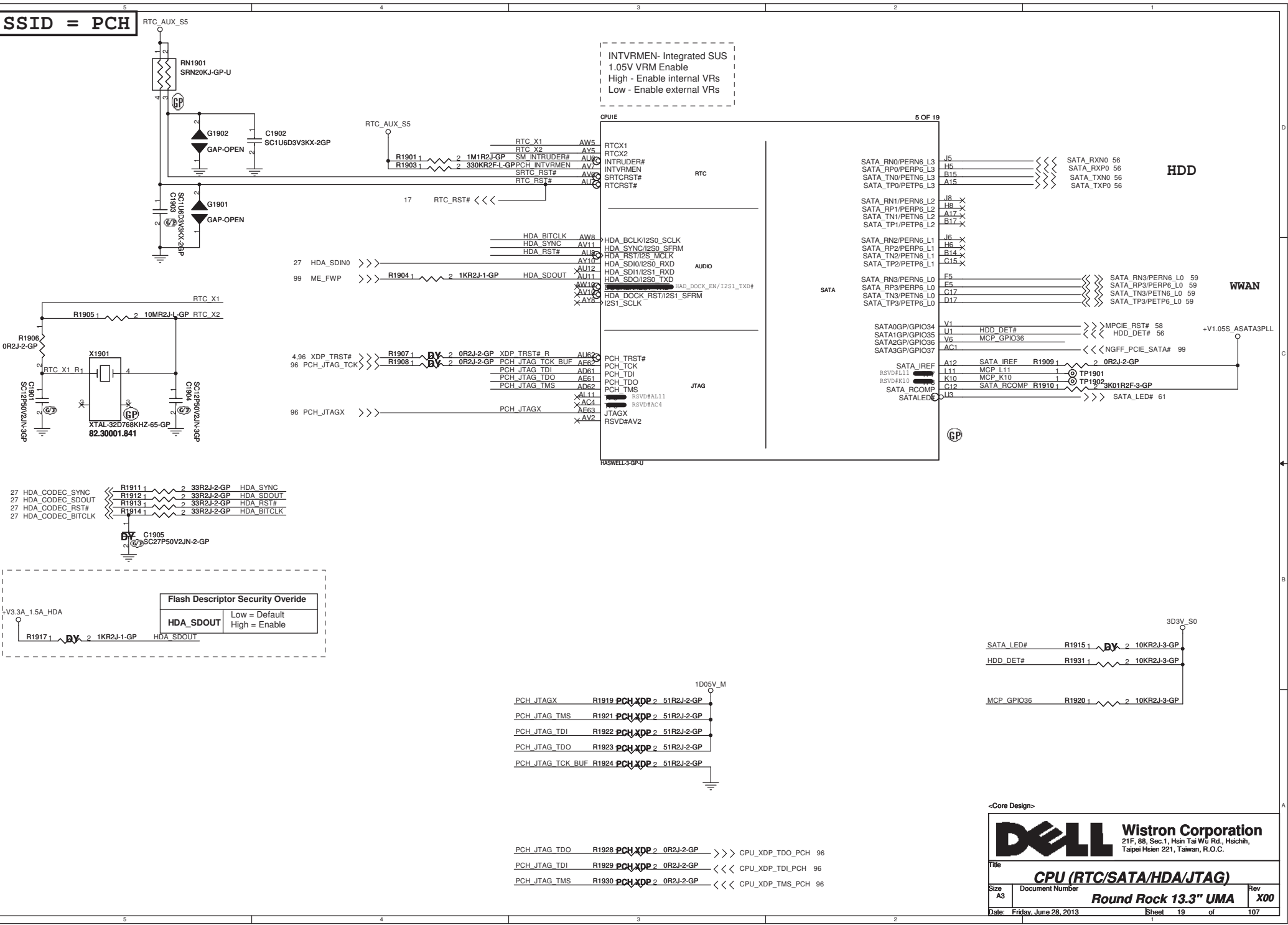
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Title: **CPU (CLOCK/SMBUS/CL/LPC/SPI)**

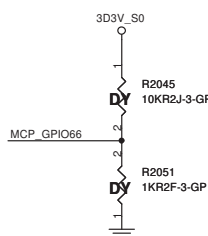
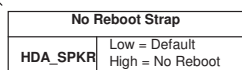
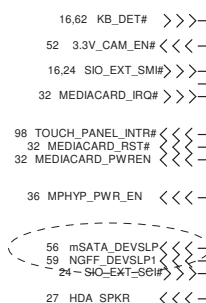
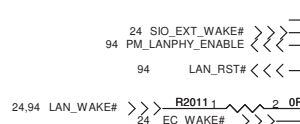
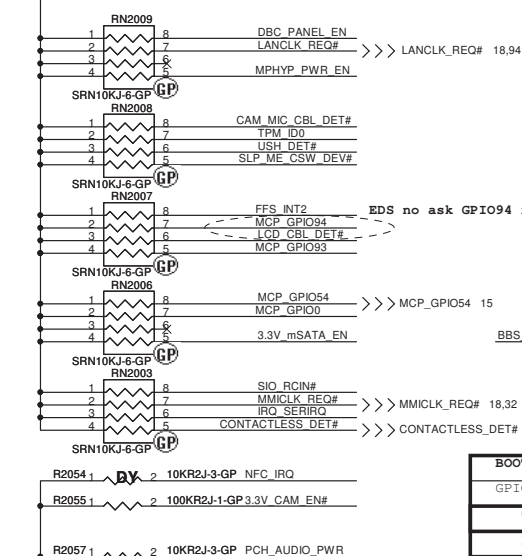
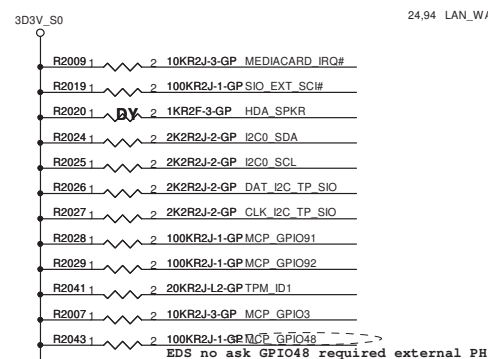
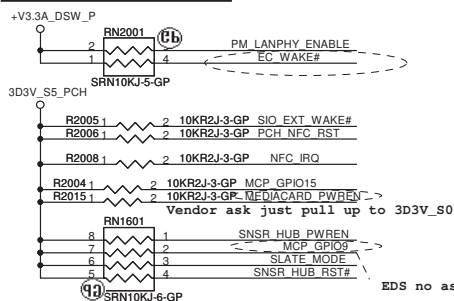
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SSID = PCH

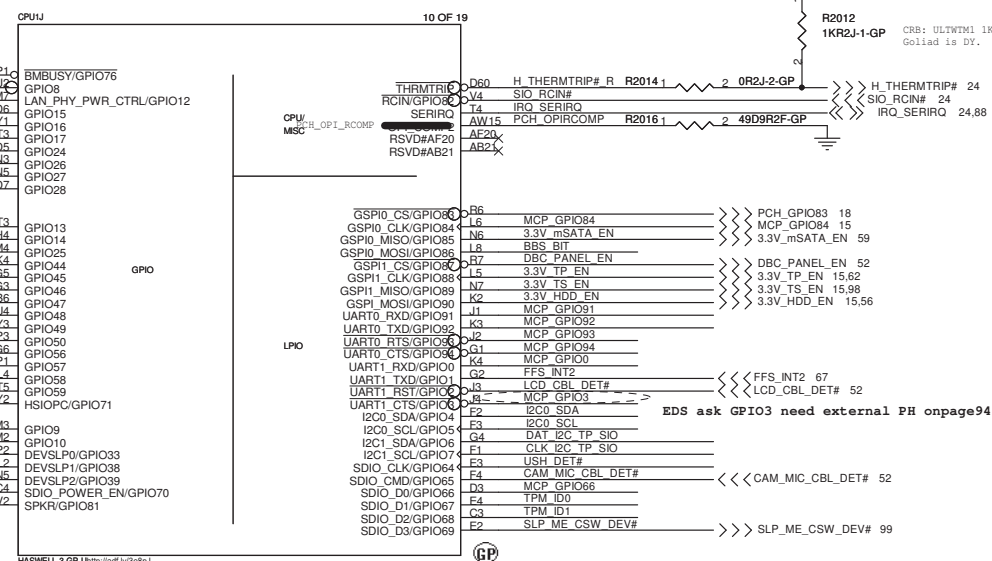


SSID = PCH



BOOT BIOS Strap	
GPIO86	BOOT BIOS Location
0	SPI (Default)
1	LPC

TOP-BLOCK SWAP OVERRIDE
GPI066
HIGH pop R20545
LOW pop R2051 (DEFAULT)

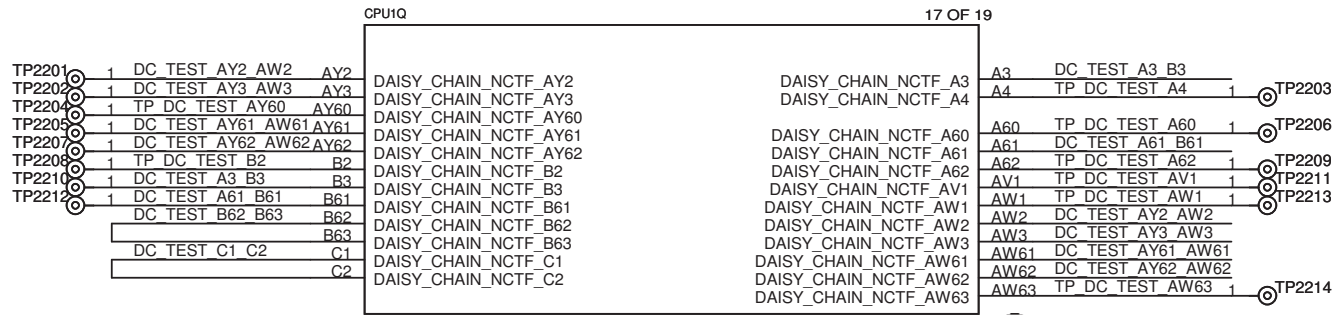


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Title			
CPU (GPIO/CPU)			
Size A3	Document Number	Round Rock 13.3" UMA	Rev X00
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Title

CPU (RSVD)

Size
A4

Document Number

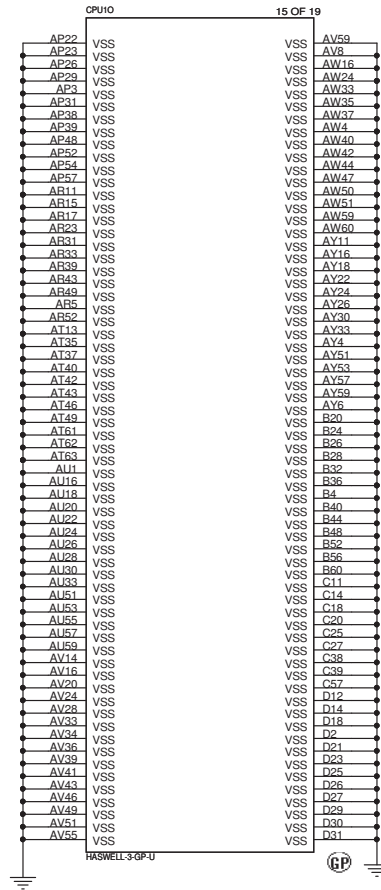
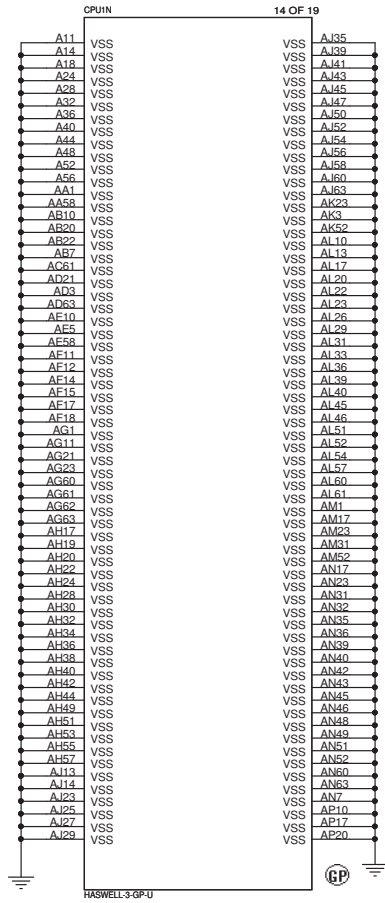
Round Rock 13.3" UMA

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SSID = PCH



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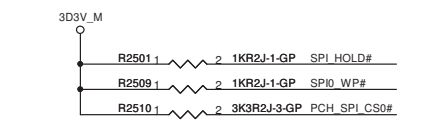


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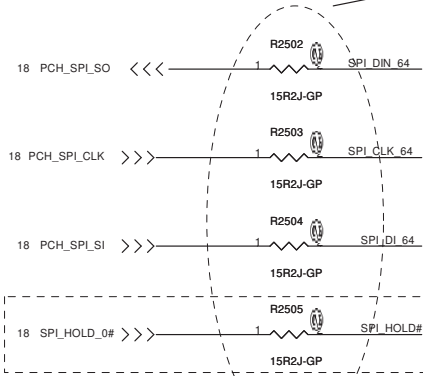
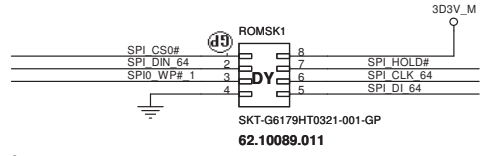
Title		CPU (VSS)	
Size	Document Number	Round Rock 13.3" UMA	
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SSID = Flash.ROM

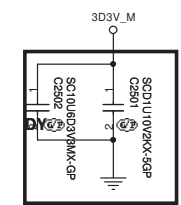
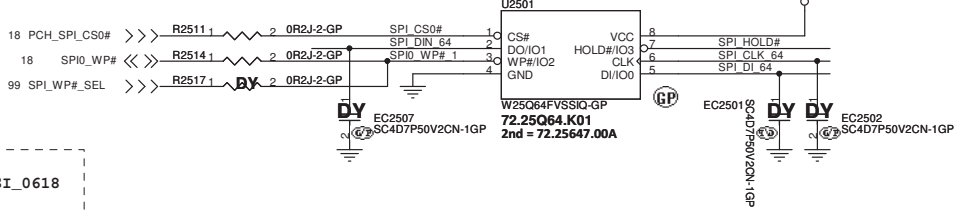
SPI ROM Equal length need to less than 500mil



Schematic Design Checklist
Single Device: 15
Multiple Devices: 33 per branch

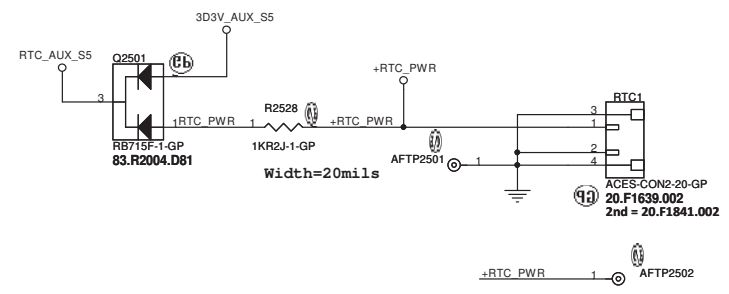


SYSTEM SPI ROM
SPI Flash ROM(8M) for PCH



Layout Note: Close to U2501 Pin 8

SSID = RTC



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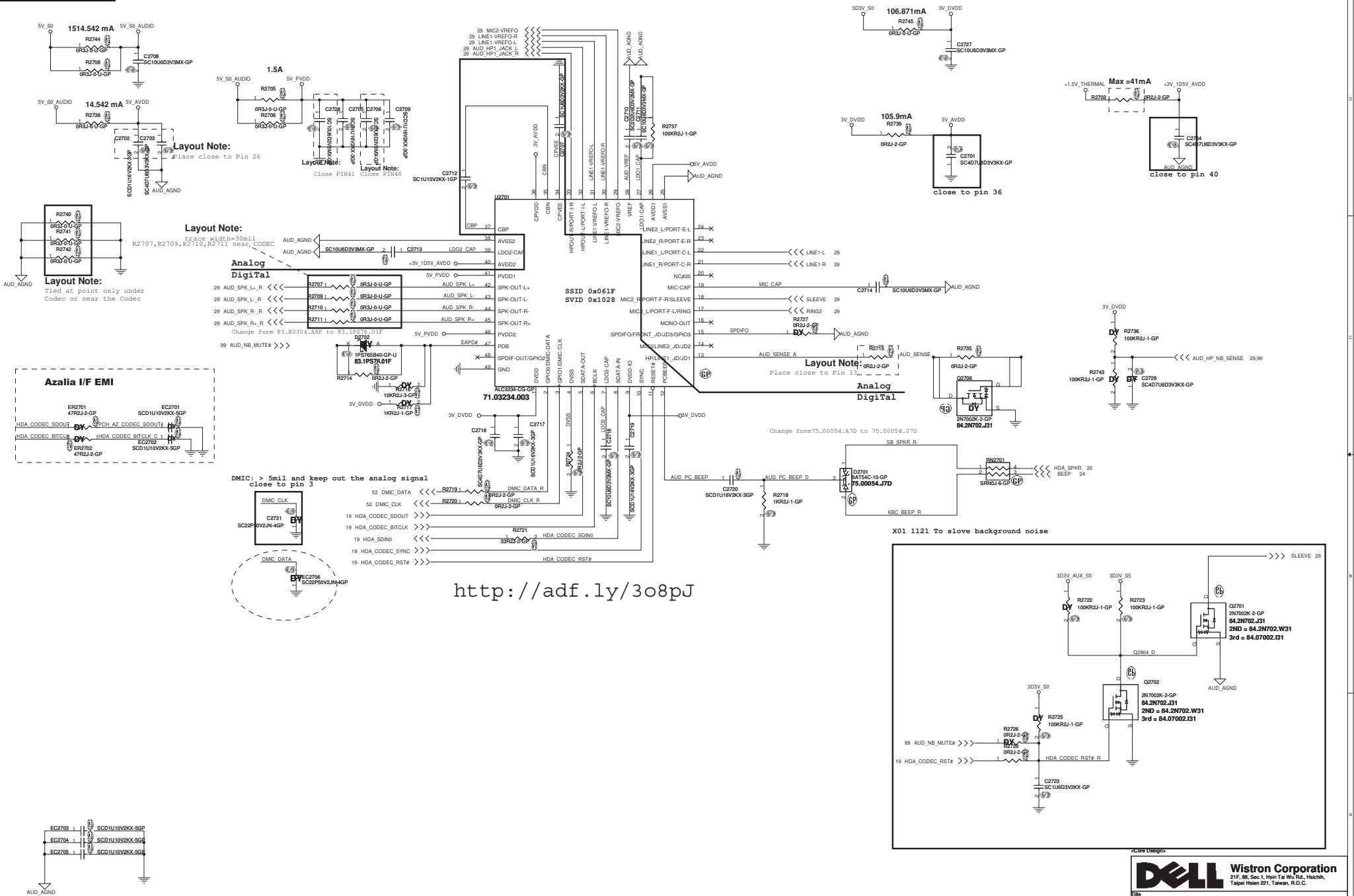
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Title **Flash/RTC**

Size A3 Document Number **Round Rock 13.3" UMAX00** Rev

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SSID = AUDIO



<http://adf.ly/3o8pJ>

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File: **Audio Codec ALC3234**
Size: **Document Number**
Date: **Friday, June 28, 2013**

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Title

Reserved

Size
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Title

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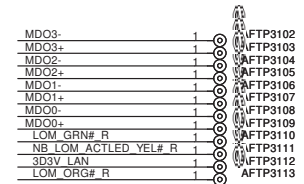
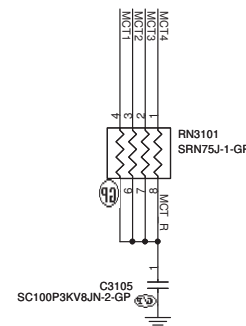
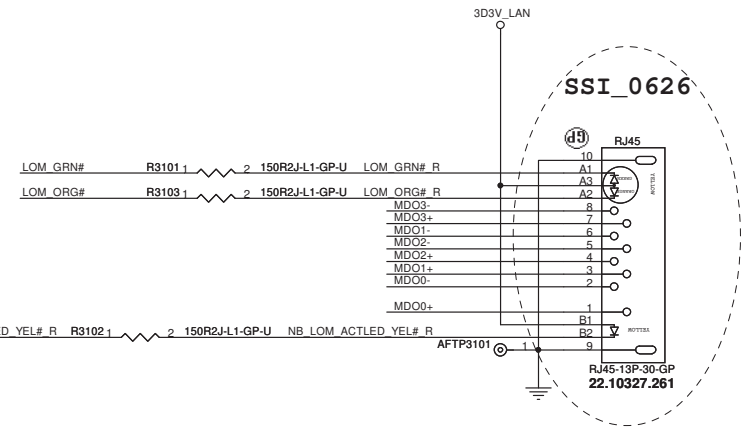
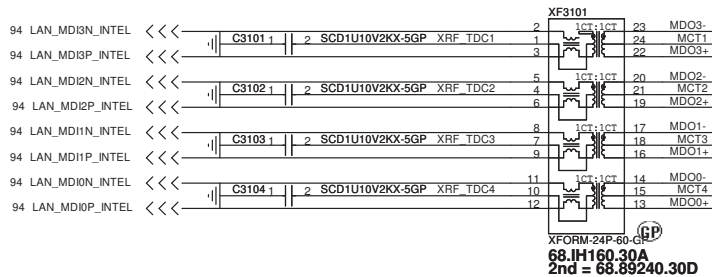
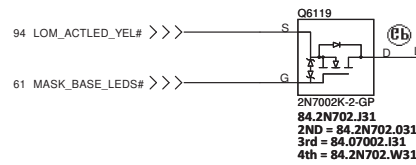
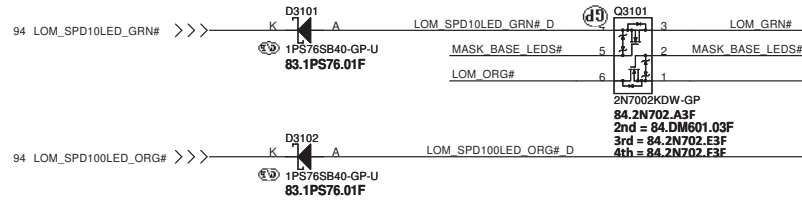
Rev

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SSID = LOM



<Core Design>

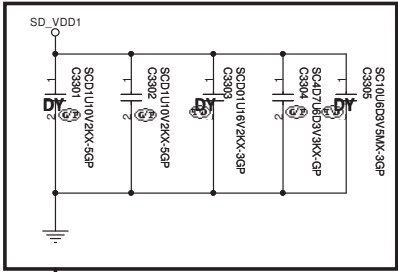
DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title **RJ45/Transformer**

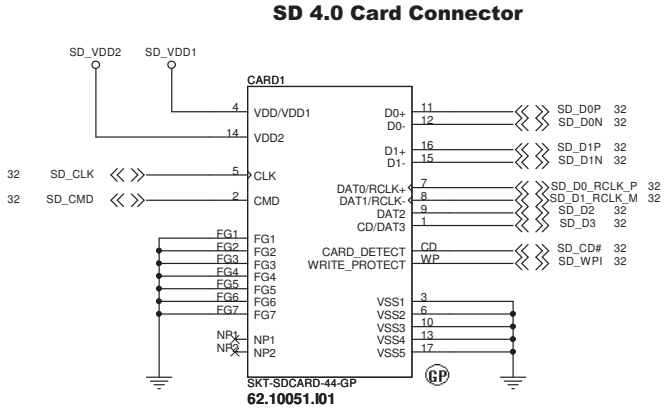
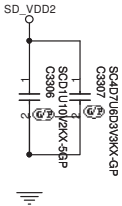
Size A3 Document Number **Round Rock 13.3" UM100** Rev

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SSID =Card Reader



Layout Note:Close to Card Reader CONN



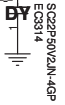
SD_CD#	1	AFTP3301
SD_D3	1	AFTP3302
SD_CLK	1	AFTP3303
SD_CMD	1	AFTP3304
SD_D0_RCLK_P	1	AFTP3305
SD_D1_RCLK_M	1	AFTP3306
SD_D2	1	AFTP3307
SD_WPI	1	AFTP3308
SD_VDD1	1	AFTP3309
SD_D0P	1	AFTP3311
SD_D0N	1	AFTP3312
SD_D1P	1	AFTP3313
SD_D1N	1	AFTP3310

SD_D3
SD_CMD
SD_D2



SD_WPI
SD_CD#
SD_D1_RCLK_M
SD_D0_RCLK_P
SD_D1N
SD_D1P
SD_D0N
SD_D0P

R3301
SD_CLK 1 2 SD_CLK C
33R2J-2-GP



SSI_0625

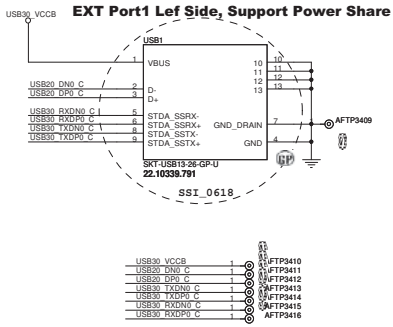
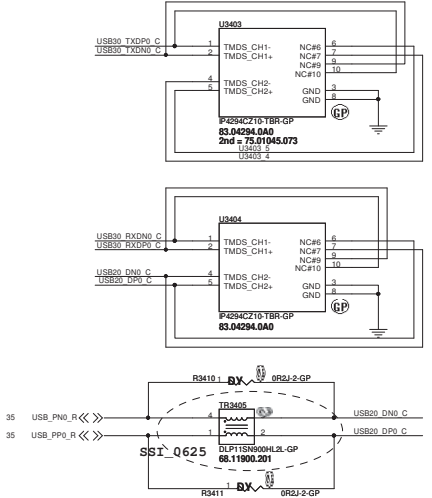
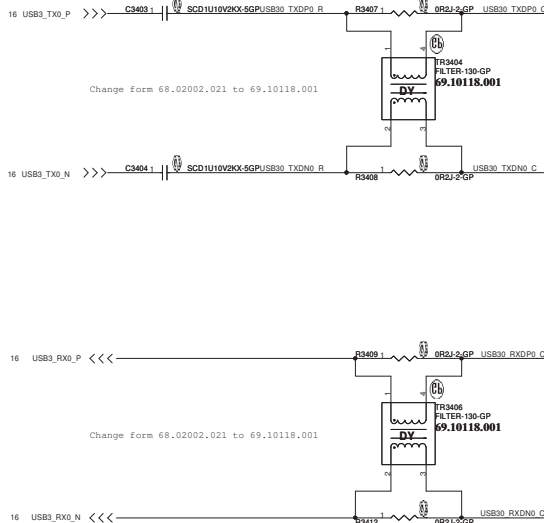
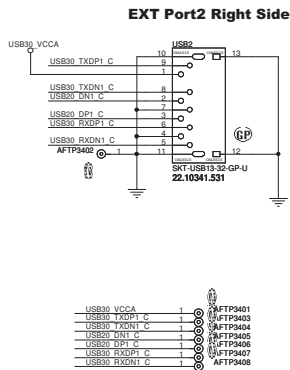
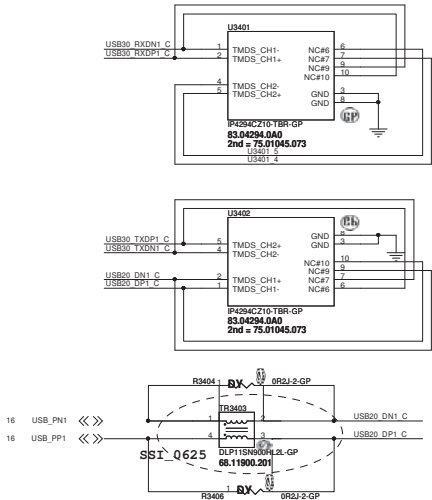
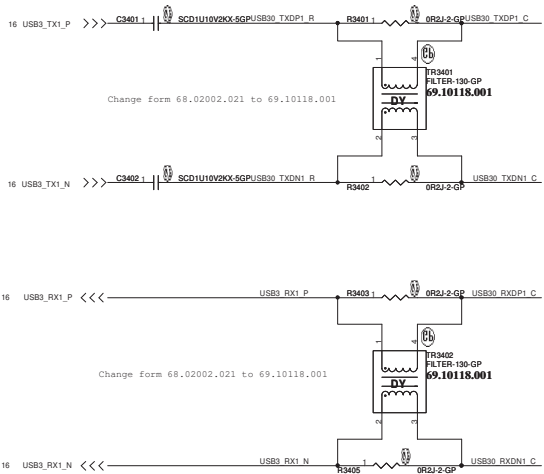
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Taipei Hsien 221, Taiwan, R.O.C.

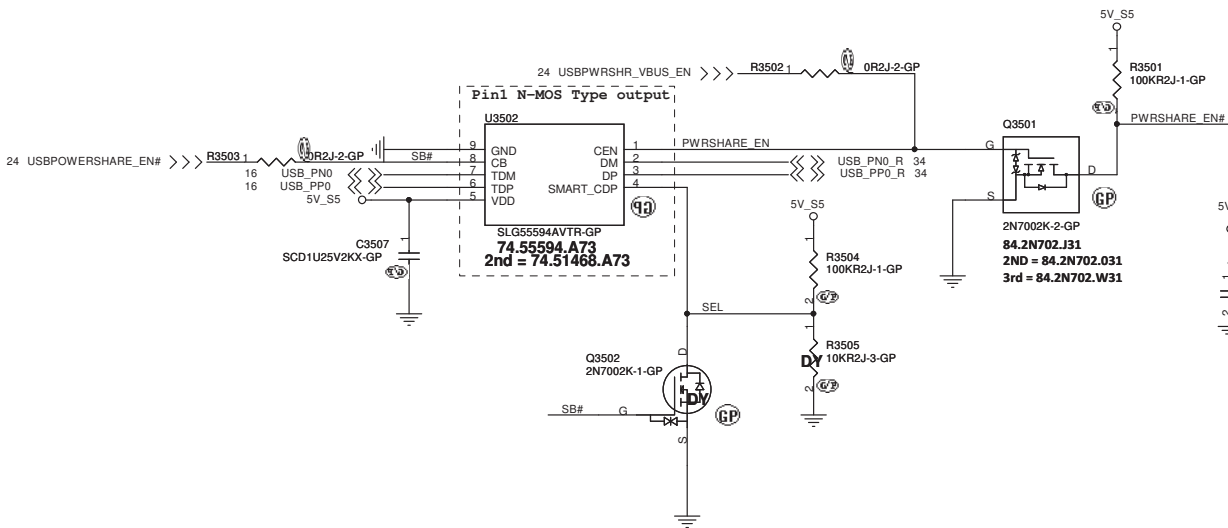
Title **Card Reader CONN**

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SSID = USB

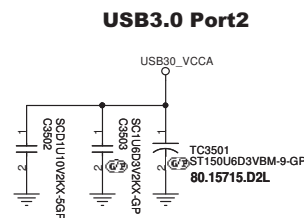
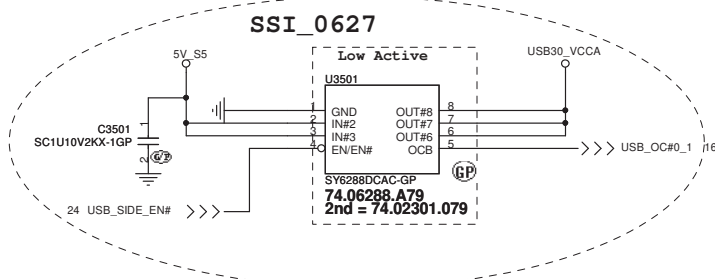


SSID = USB



USB Power SW (U3501 & U3503)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.079	2ND
			3RD



<Core Design>



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Title

USB3.0 Power SW

Size

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5 4 3 2 1

SSID = Reset.Suspend

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<Core Design>



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Title

S3 Reduction

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<Core Design>



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Title

Reserved

Size
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SSID = OBFF

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Title

Reserved

Size
A

Document Number

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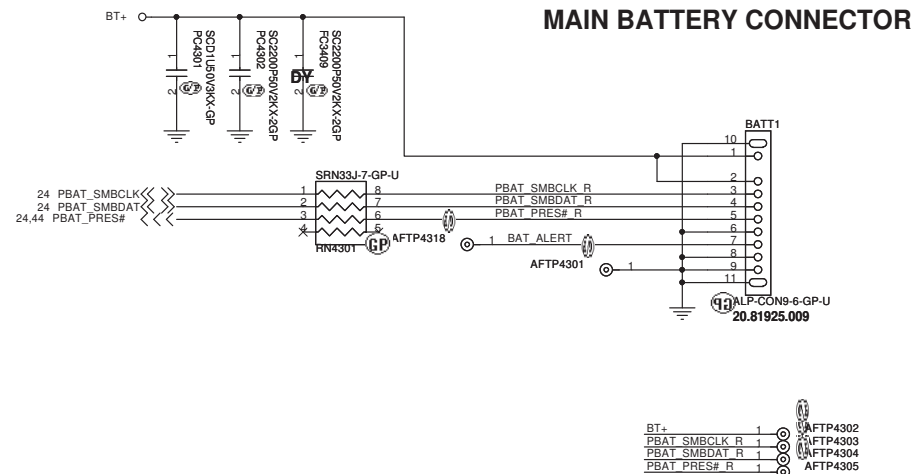
Rev

X00

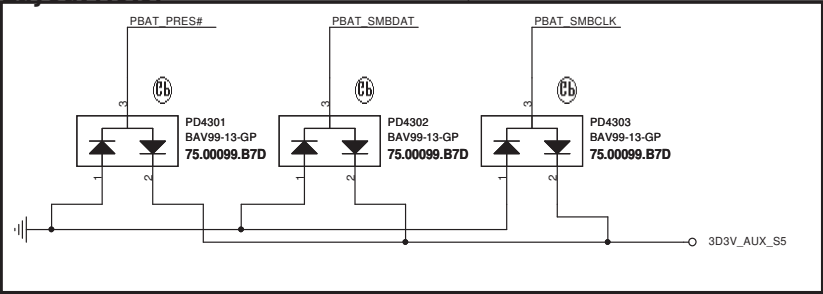
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SSID = PWR.Support



Layout Note: Place near Battery CONN



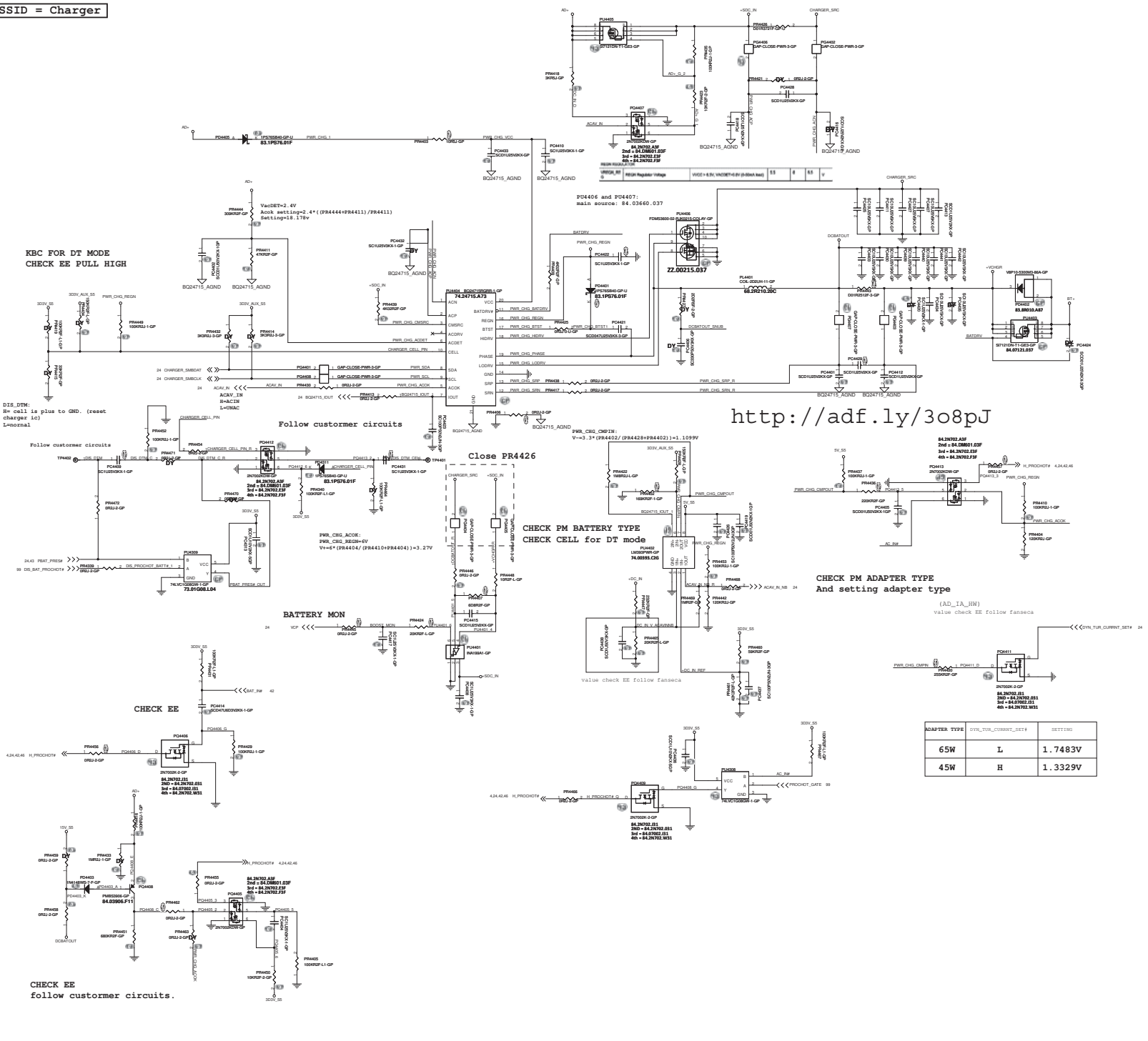
<Core Design>

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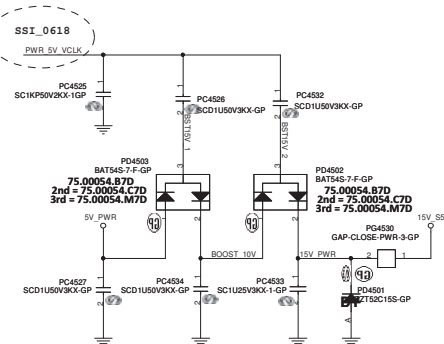
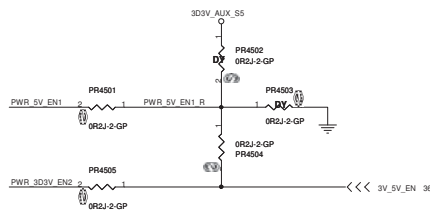
BATTERY CONN

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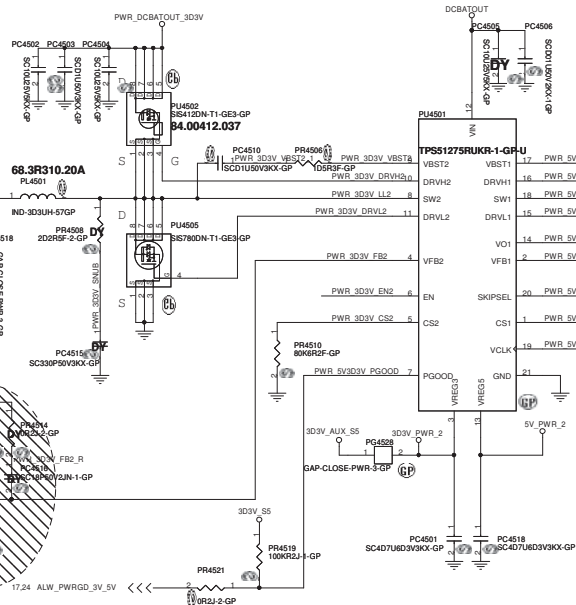
SSID = Charger



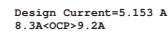
SSID = PWR.Plane.Regulator_5v3p3v



Design Current=5.894 A
8.841A<OCP>10.6A



SSI need to change to polymer cap



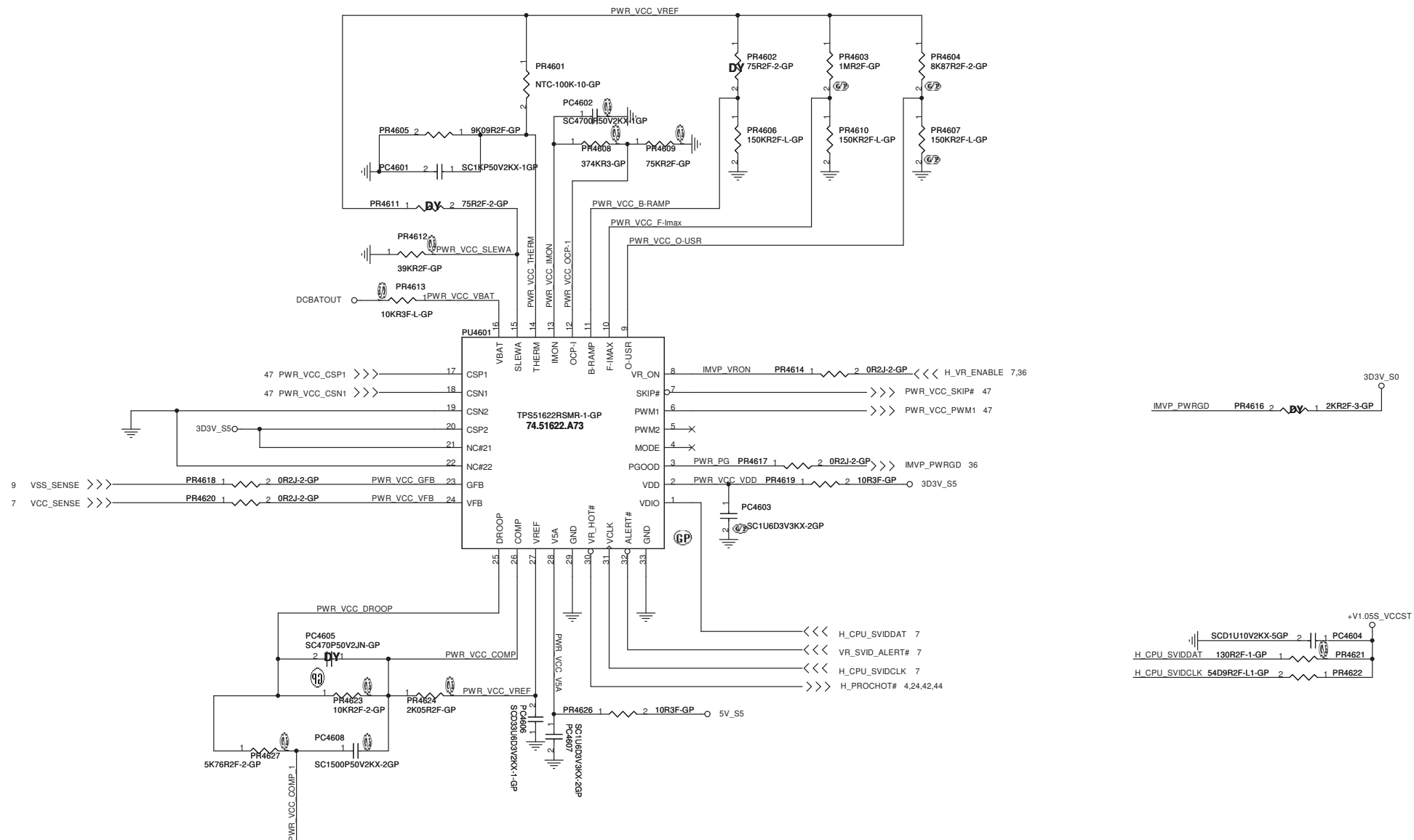
SSI need to change to polymer cap

Close to VFB Pin (pin2)

I/P cap: CHIP CAP C 1 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC037-3R3MN Cyntec 28mhm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsui/ 17mOhm / 77.52271.09L
H/S:SI412DN-T1-GE3 / 24mohm/30mOhm4A.5Vgs / 84.00412.037
L/S:SI406DN-T1-GE3 / 11.5mOhm/14.5mOhm4A.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 10U 25V K0805 X3R/ 78.10622.51L
Inductor: CHIP IND 3.3UH P3CMV06T3-3R3M Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SI1421D2N-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SI1406D2N-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

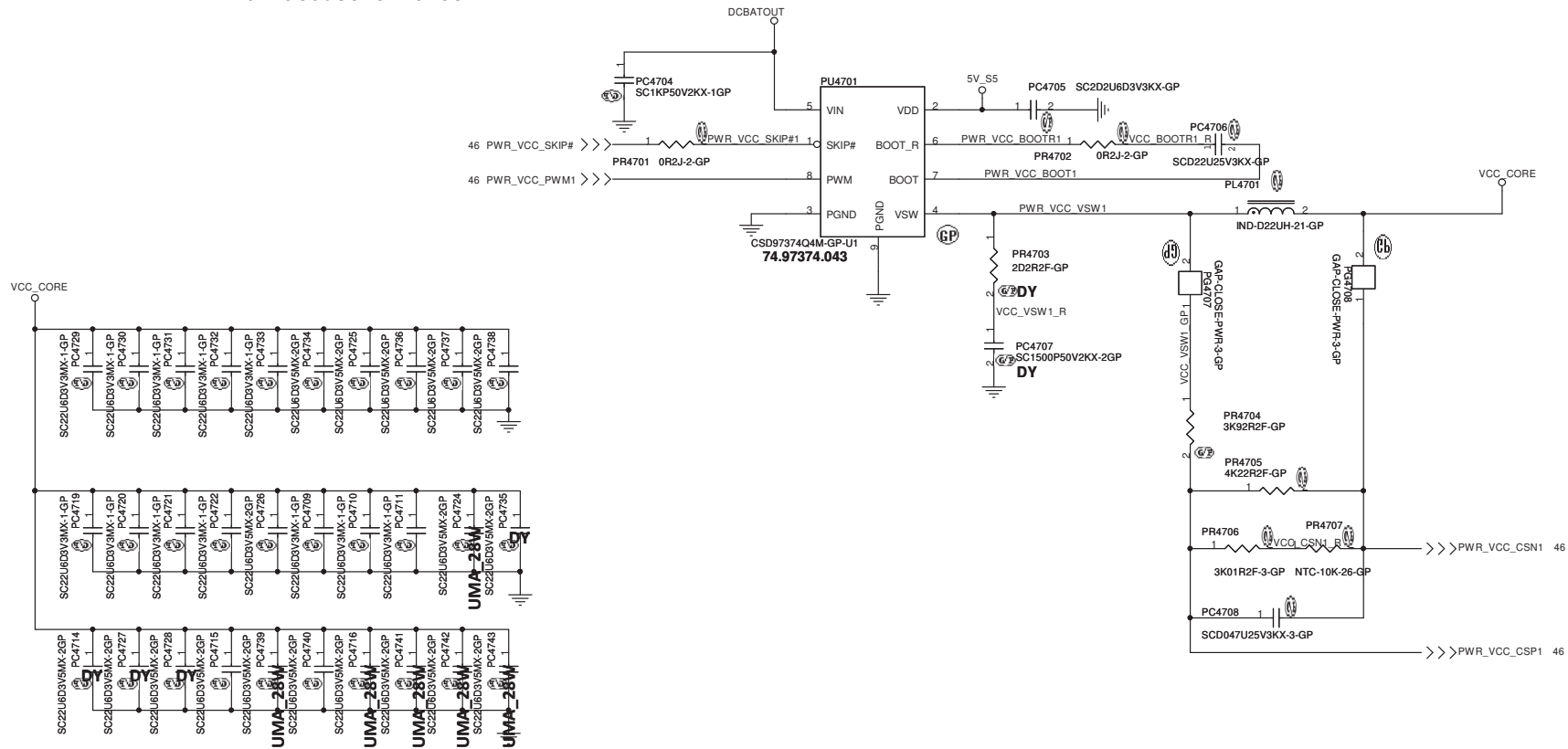
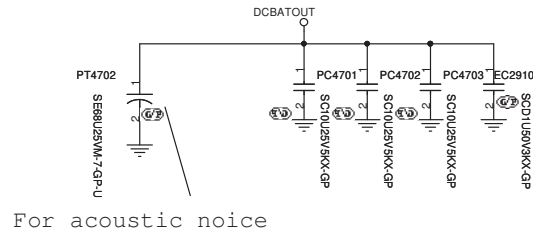
SSID = CPU.Regulator



<Core Design>

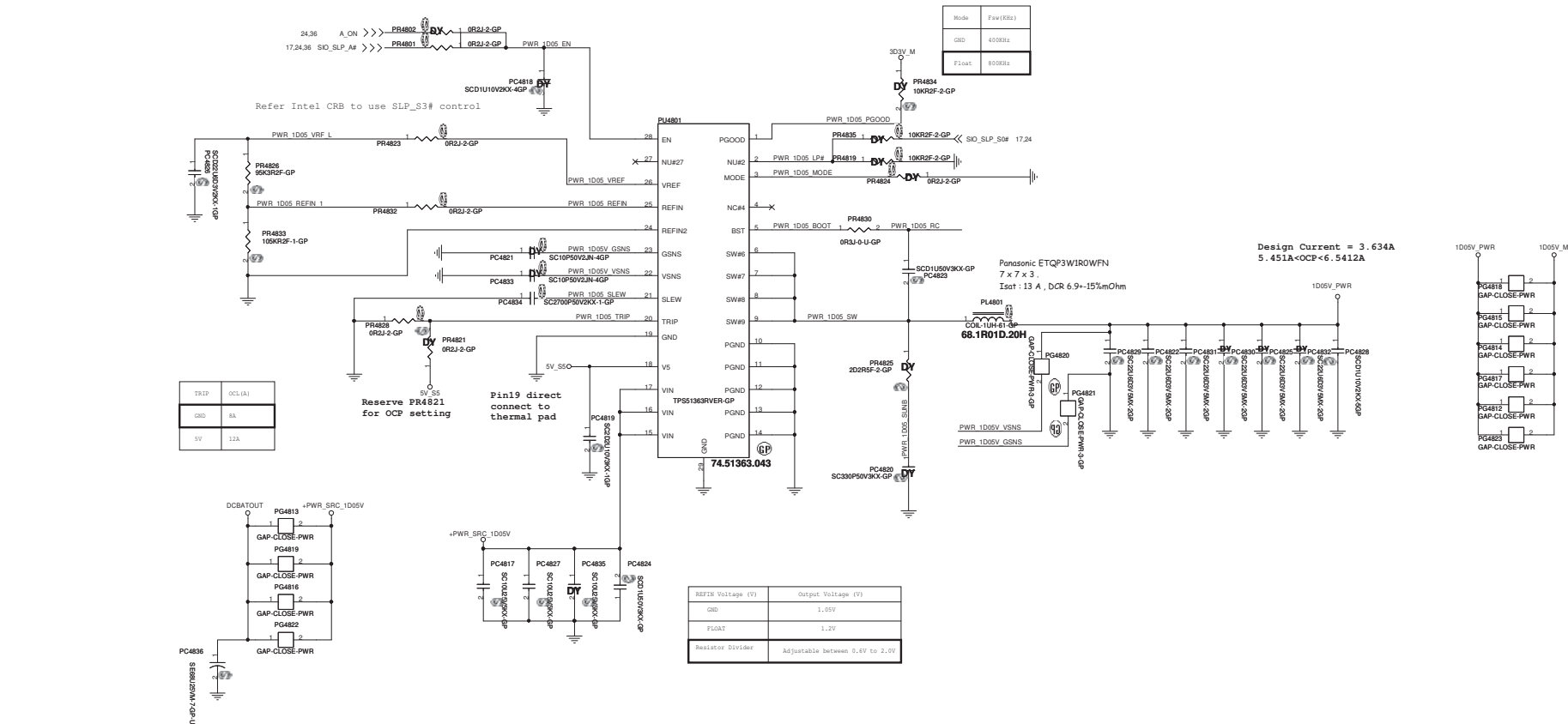
DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title TPS51622 CPUCORE(1/2)		
Size A3	Document Number	Rev X00
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SSID = CPU.Regulator

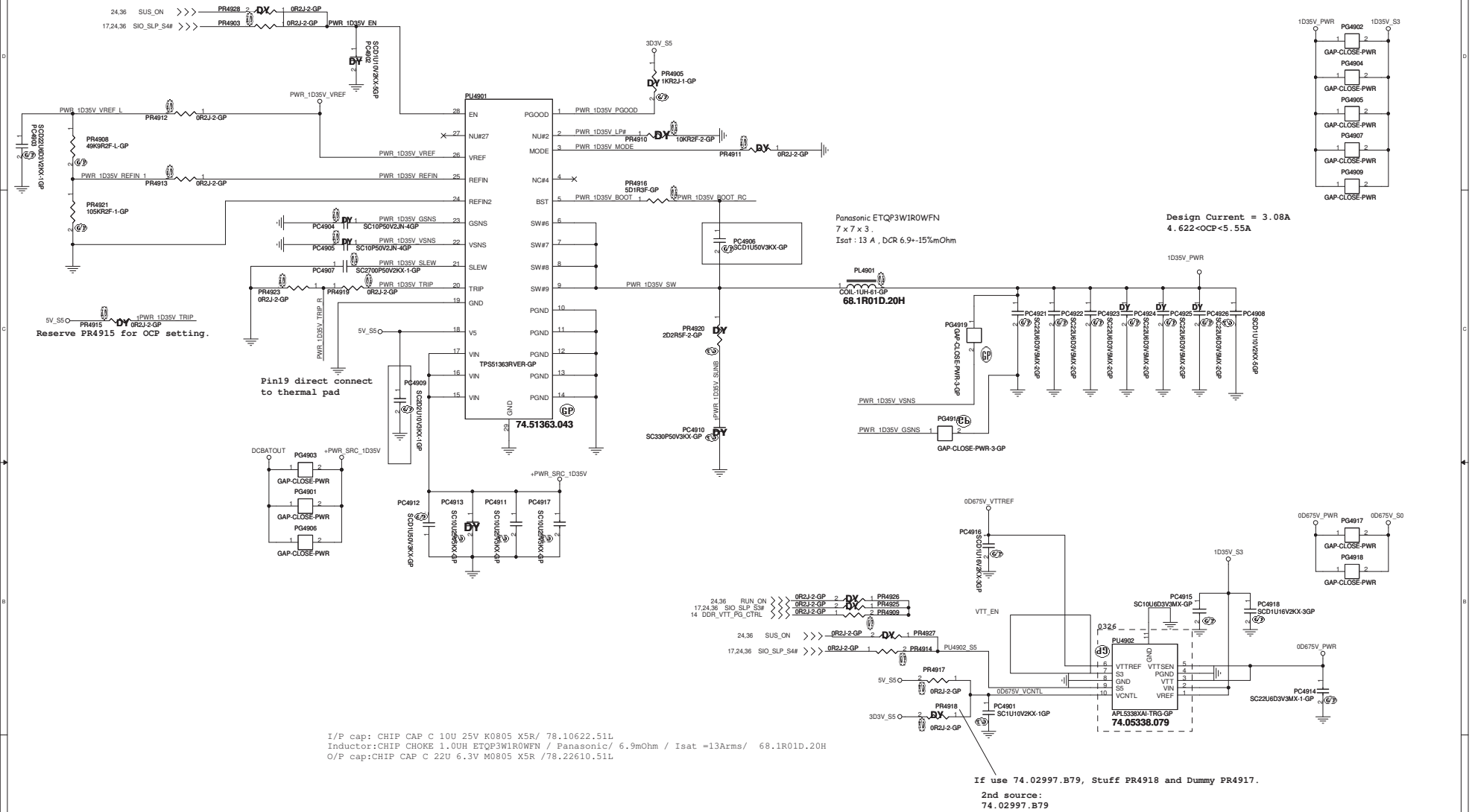


<Core Design>

DELL		Wistron Corporation	
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Title		TPS51622 CPUCORE(2/2)	
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SSID = PWR.Plane.Regulator lp35v0p675v



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File
TPS51363+5338 1D35V & 0D675V

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<Core Design>



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Title

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Title

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Size
A4

Document Number

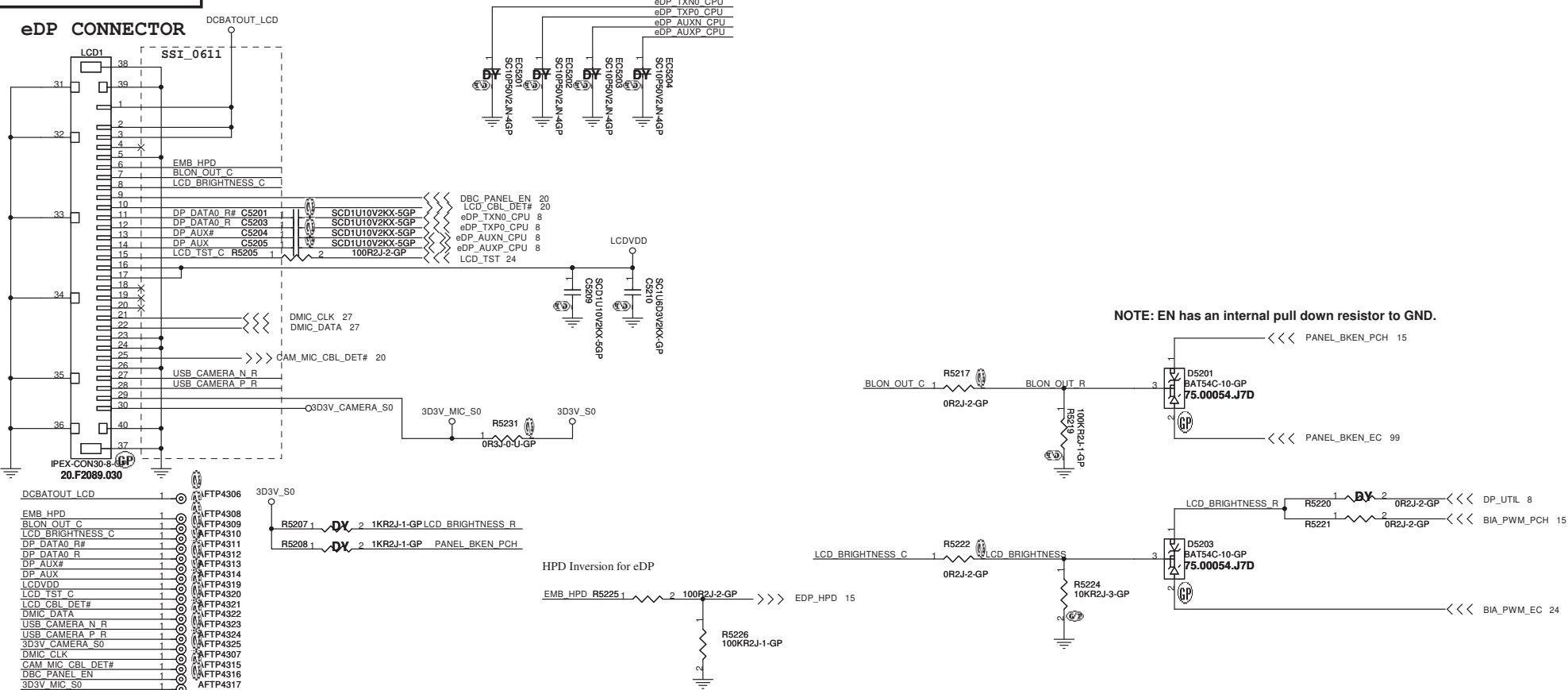
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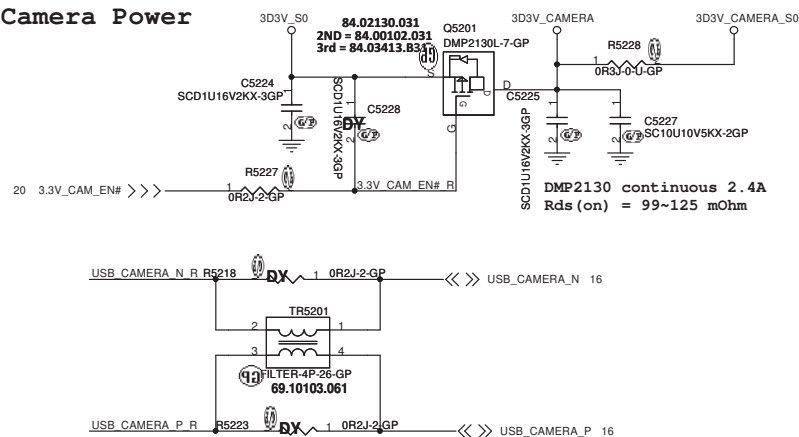
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SSID = VIDEO

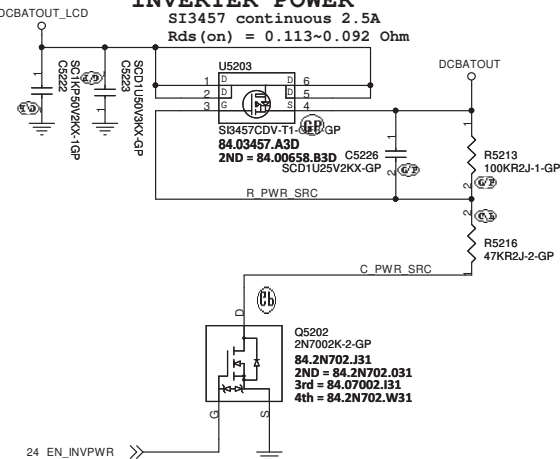


Camera Power



INVERTER POWER

SI3457 continuous 2.5A

$$R_{ds(on)} = 0.113 \sim 0.092 \text{ Ohm}$$


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Title			
eDP Connector			
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Title

Reserved

Size
A4

Document Number

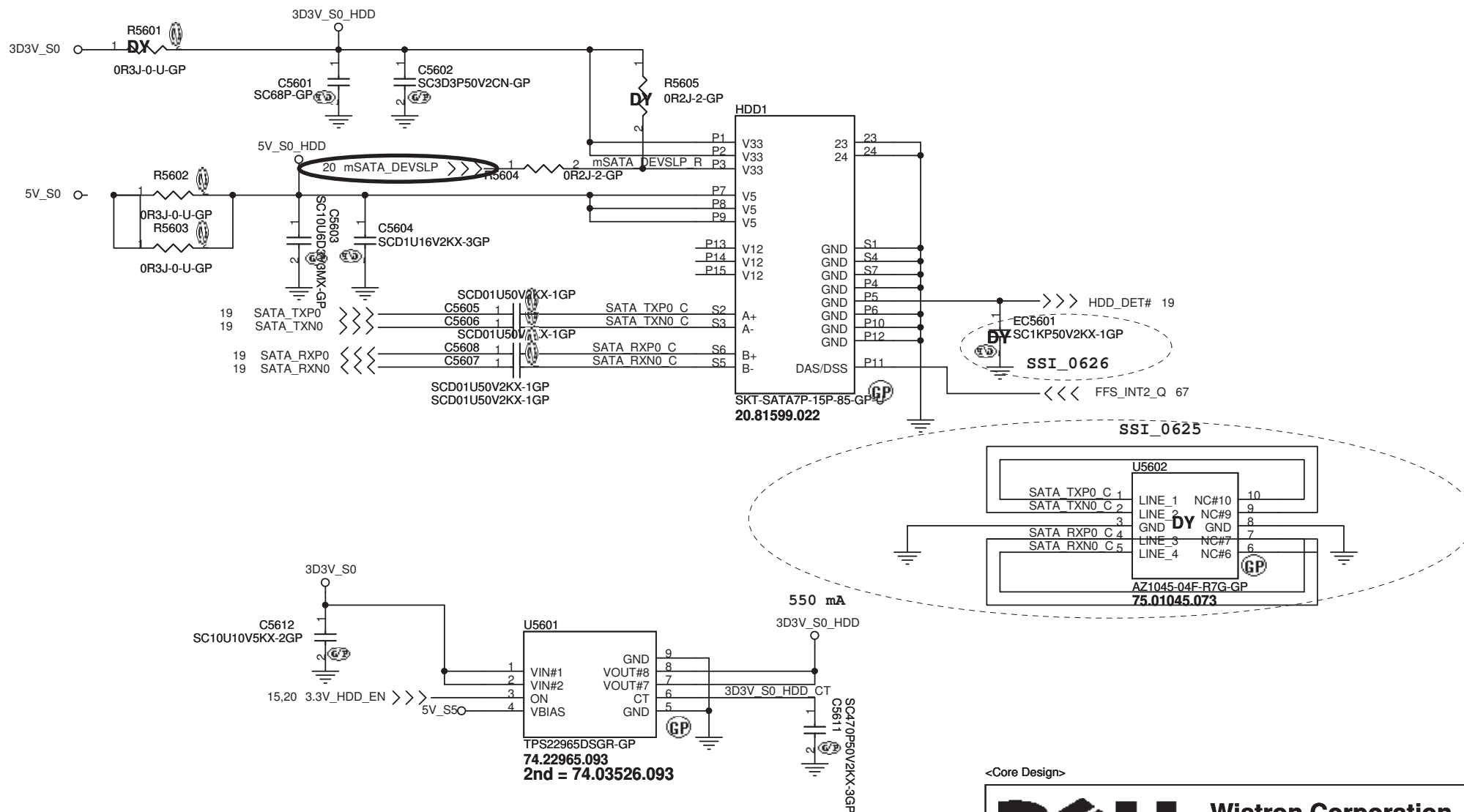
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SSID = SATA



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Title

HDD

Size
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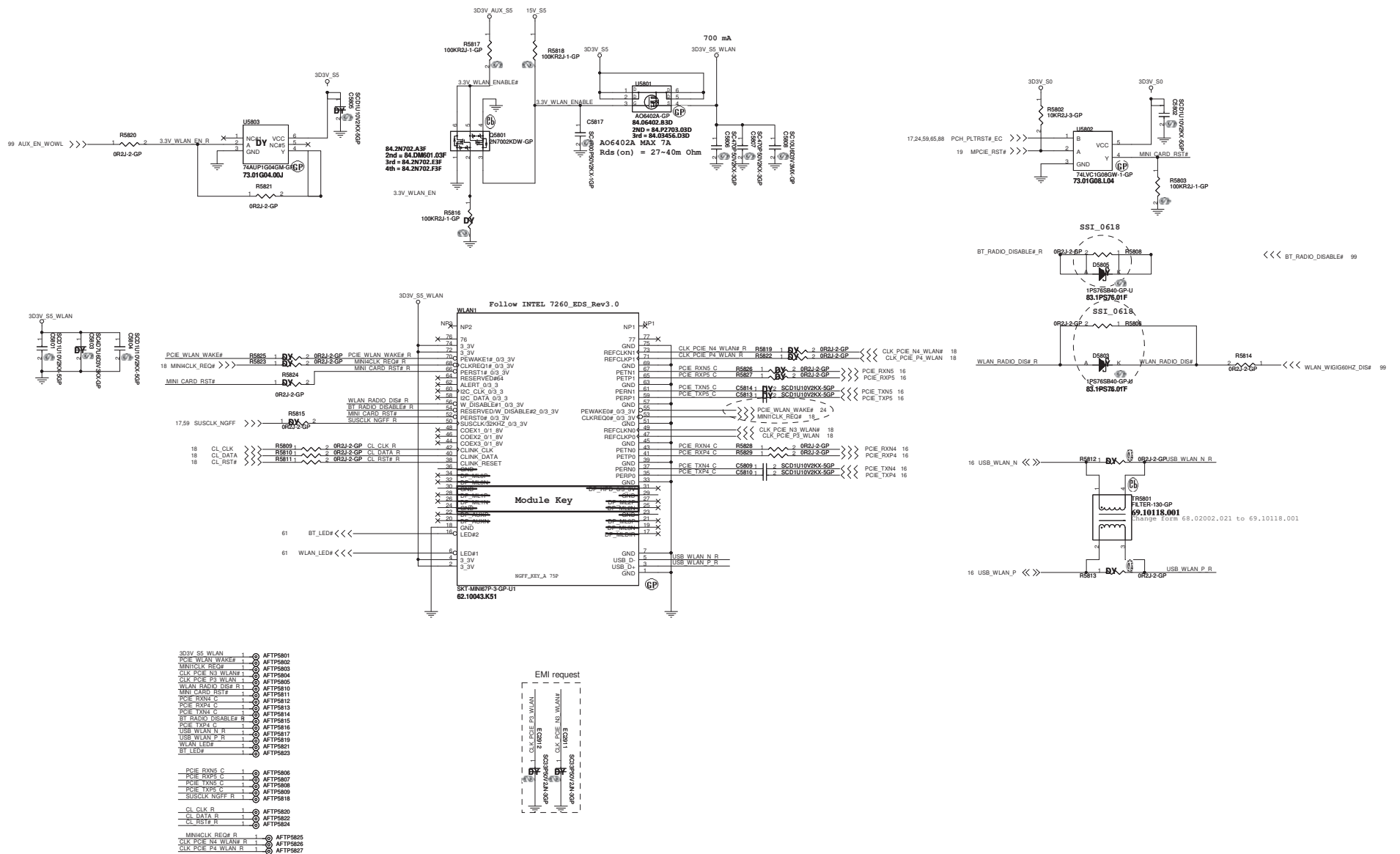
Title

Reserved

Size A4	Document Number	Rev X00
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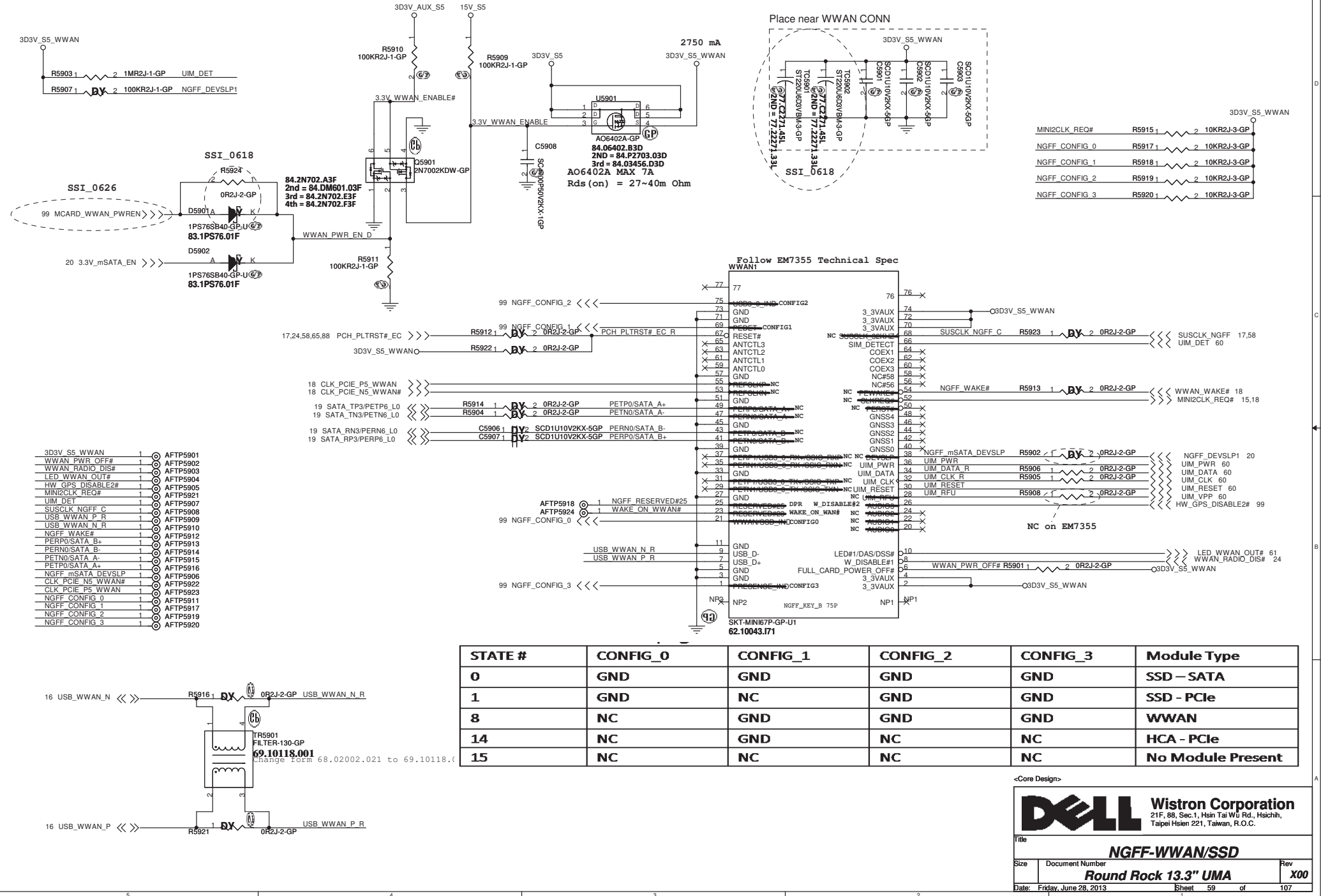
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SSID = WIRELESS

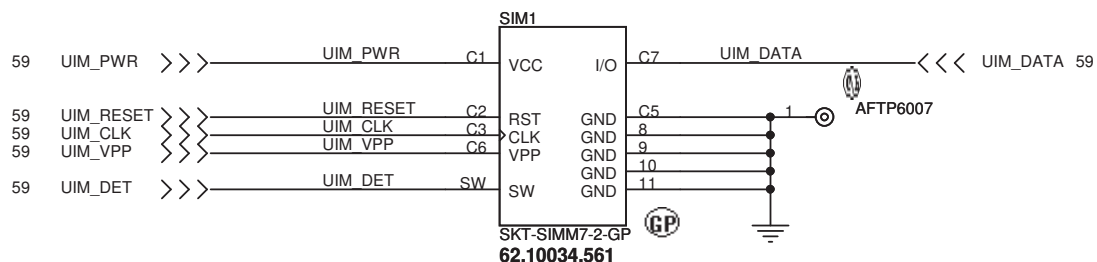


SSID = WIRELESS

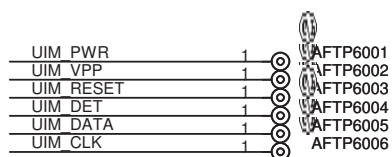
NGFF(WWAN/SSD)



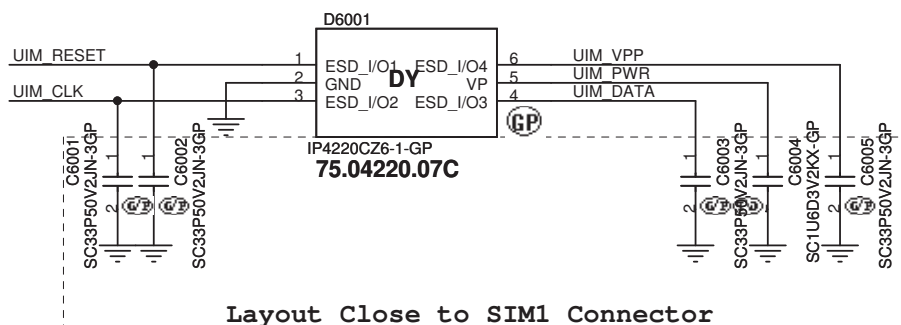
SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



Change from 83.00005.BAE to 75.04220.07C



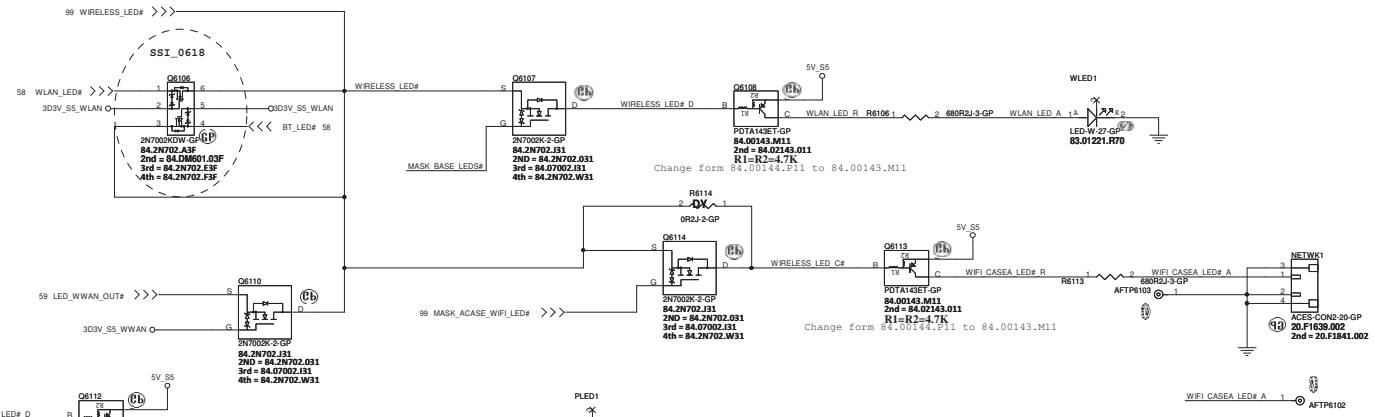
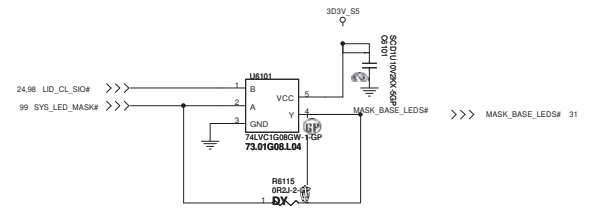
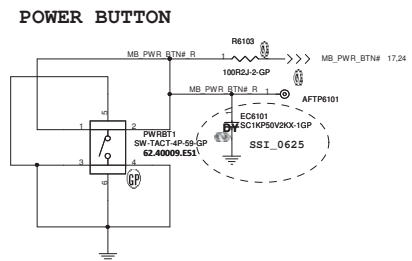
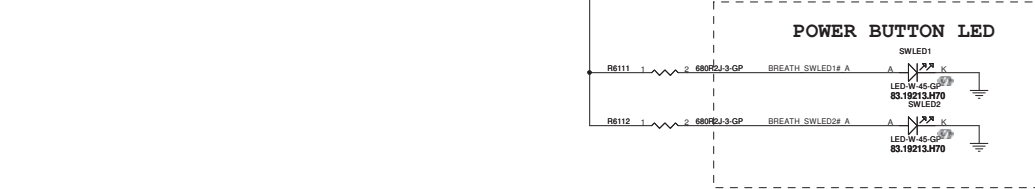
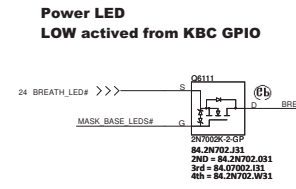
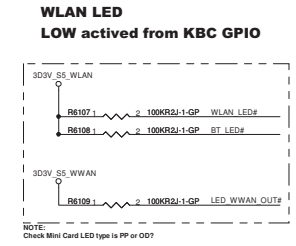
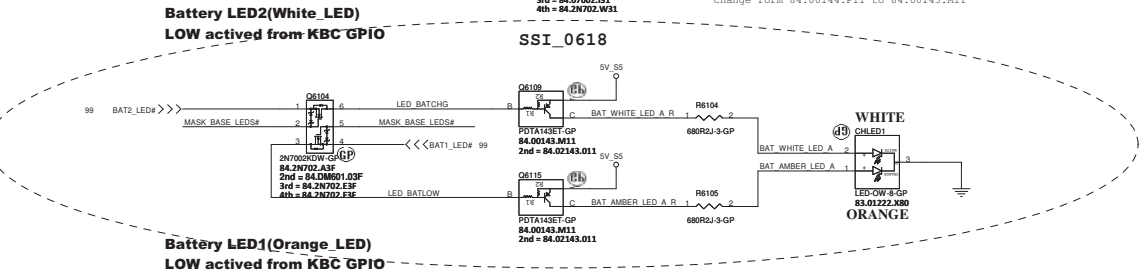
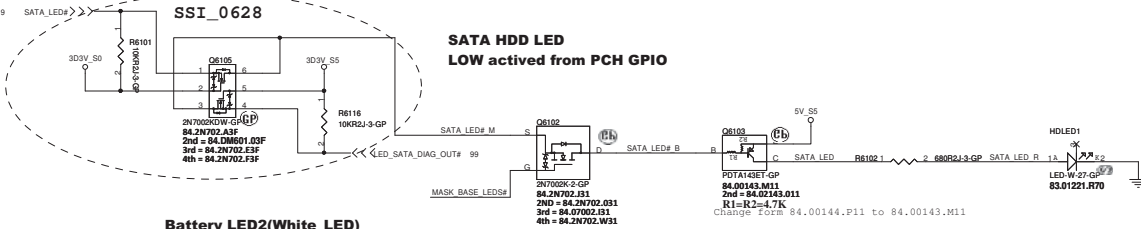
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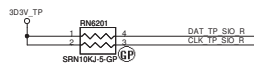
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Title		
mSATA		
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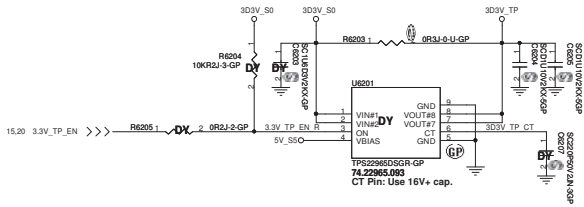
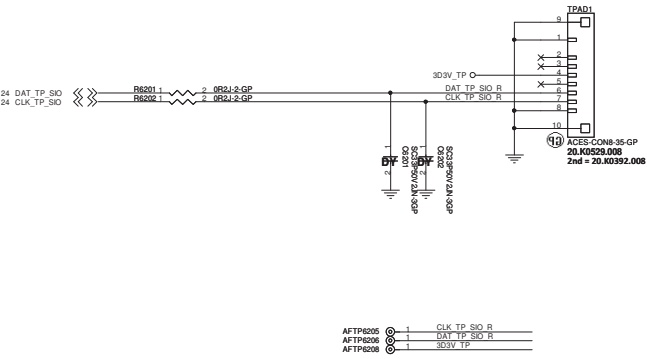
SSID = User.Interface



SSID = KBC SSID = Touch.Pad

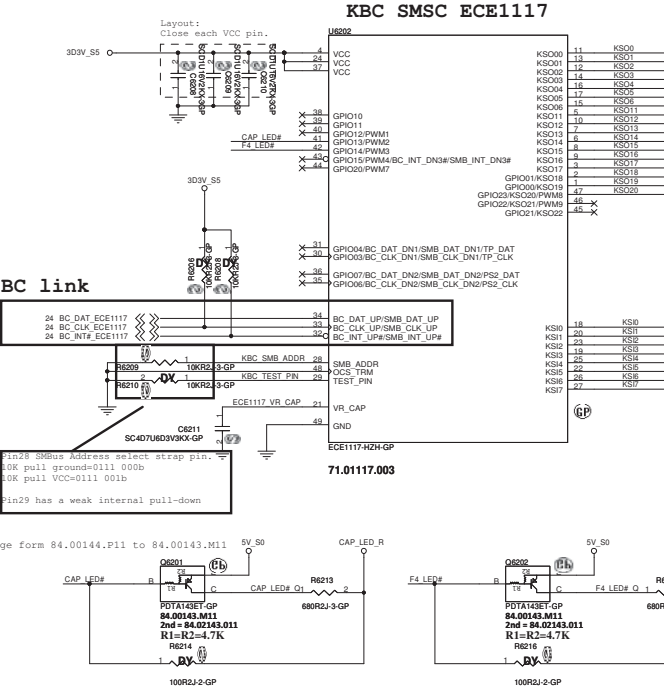
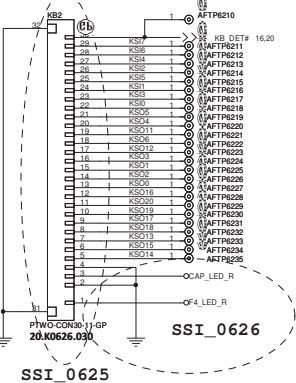


TouchPad Connector



MB Pin NO.	Description	Module Pin NO.
30	Diagnostic	1
29	KSI[7]:S8	2
28	KSI[6]:S7	3
27	KSI[4]:S5	4
26	KSI[2]:S3	5
25	KSI[5]:S6	6
24	KSI[1]:S2	7
23	KSI[3]:S4	8
22	KSI[0]:S1	9
21	KSO[5]:D6	10
20	KSO[4]:D5	11
19	KSO[11]:D8	12
18	KSO[6]:D7	13
17	KSO[12]:D9	14
16	KSO[3]:D4	15
15	KSO[1]:D2	16
14	KSO[2]:D3	17
13	KSO[0]:D1	18
12	KSO[16]:D13	19
11	KSO[20]:D17	20
10	KSO[19]:D16	21
9	KSO[17]:D14	22
8	KSO[18]:D15	23
7	KSO[13]:D10	24
6	KSO[15]:D12	25
5	KSO[14]:D11	26
4	GND	27
3	Caps Lock LED	28
2	GND	29
1	F4 LED	30

Internal KeyBoard Connector



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Key Board/Touch Pad
Round Rock 13.3" UMA
Date: Friday, June 26, 2013

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Title

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Size
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Title

Hall Sensor

Size

Document Number

Round Rock 13.3" UMA

Rev

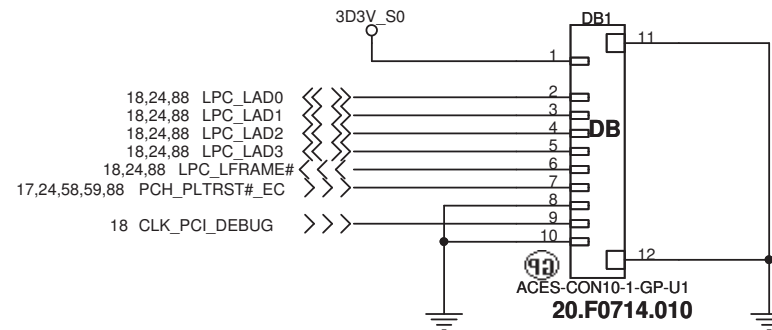
X00

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SSID = DEBUG PORT

SB modify to test pad



<Core Design>



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Title

Debug connector

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<Core Design>



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Title

Thunderbolt (1/5)

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<Core Design>



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Title

Thunderbolt (2/5)

Size
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<Core Design>



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Title

Thunderbolt (3/5)

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<Core Design>



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Title

Thunderbolt (4/5)

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Title

Thunderbolt (5/5)

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<Core Design>



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Title

GPU (1/5) PEG

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Title

GPU (2/5) DIGITAL

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<Core Design>



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Title

GPU (3/5) VRAM

Size
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<Core Design>



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Title

GPU (4/5) GPIO

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Title

GPU (5/5) PWR/GND

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Title

VRAM1,2 (1/4)

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Title

VRAM3,4 (2/4)

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Title

VRAM5,6 (3/4)

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Title

VRAM7,8 (4/4)

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Title

VGA CORE

Size
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Title

DISCRETE VGAPOWER

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Title

Switchable GFXLCD

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Title

Switchable GFXCRT

Size
A

Document Number

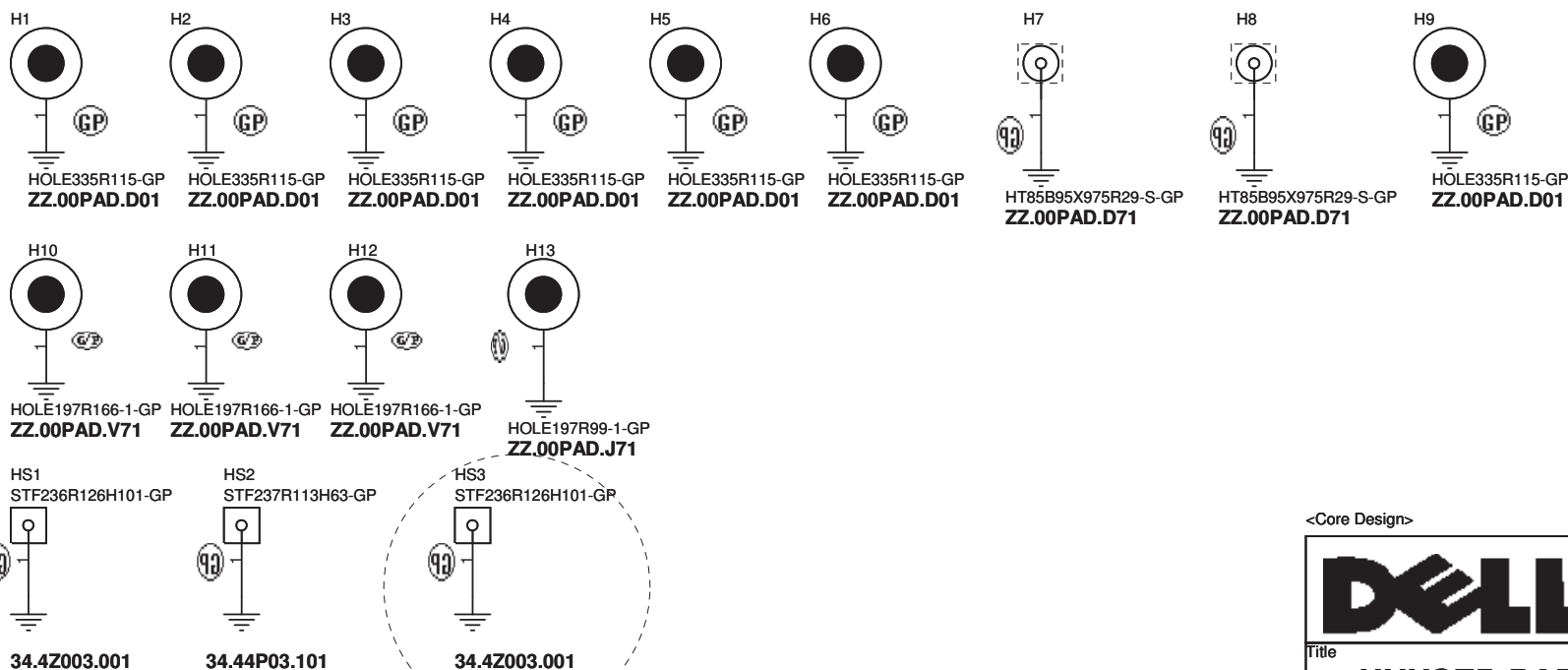
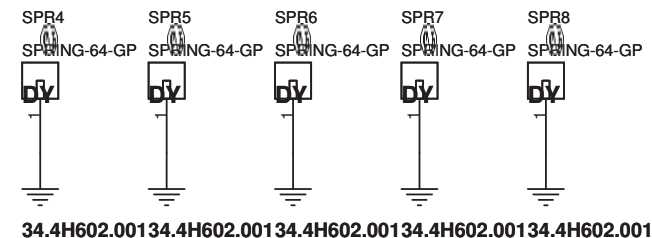
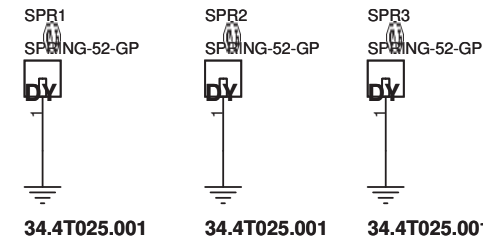
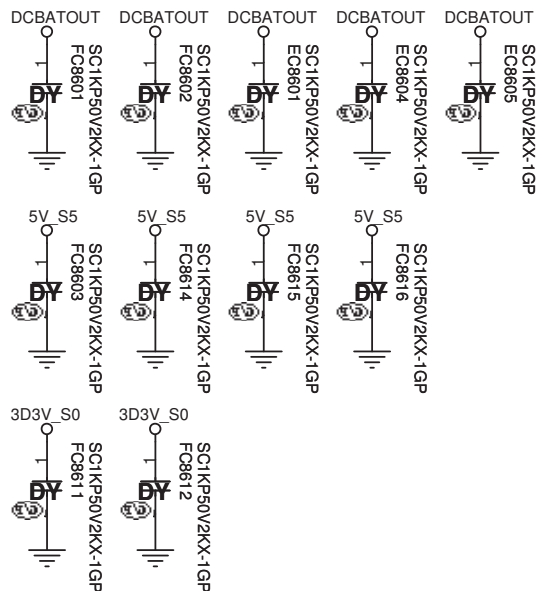
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SSID = USH

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<Core Design>



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Title

USH Board Connector

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<Core Design>



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Finger Print

Size
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<Core Design>



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Title

NFC Connector

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<Core Design>



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Title

Smart Card

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<Core Design>



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Title

Reserved

Size
A

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SSID = Docking

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<Core Design>



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Title

DOCKING

Size
A4

Document Number

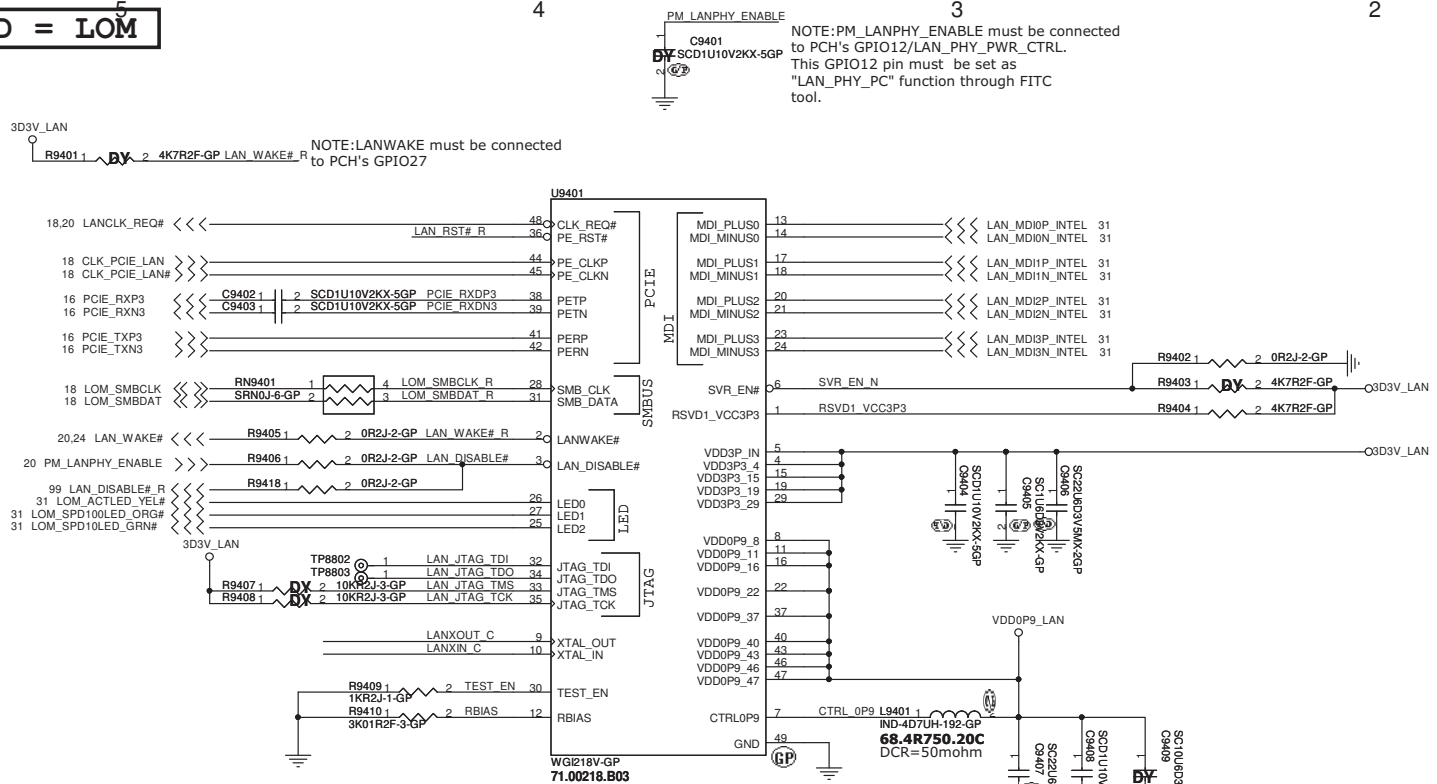
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SSID = LOM

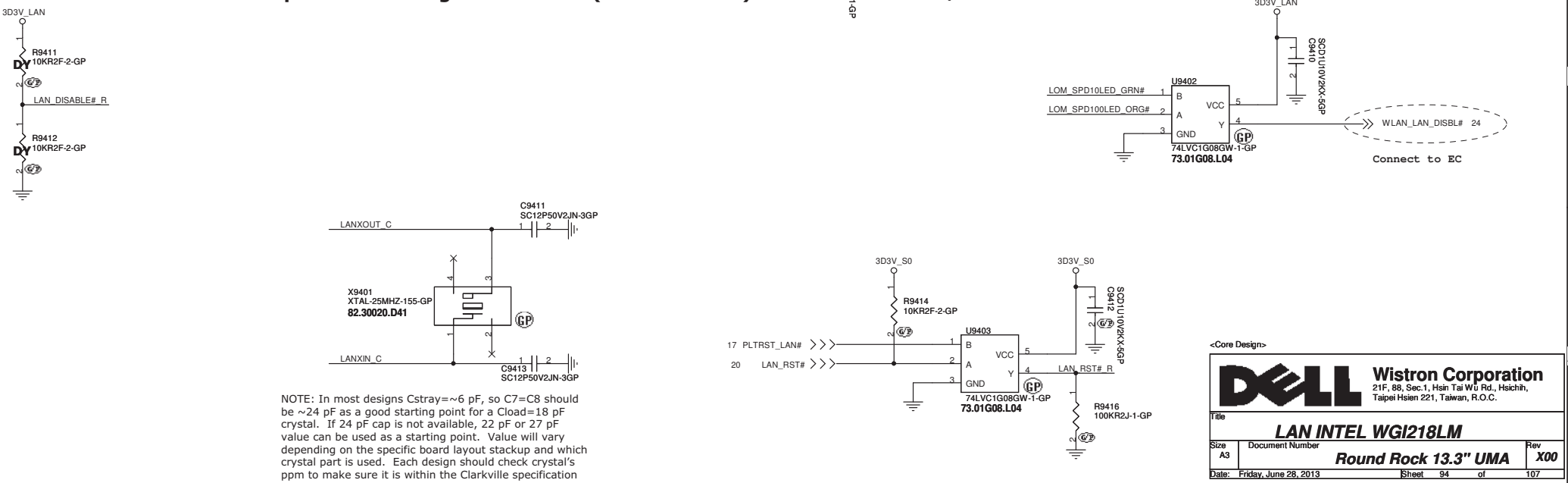


0D9V Power Options
SVR_EN_N: Pull High External
Pull Low Internal

Internal SVR	Shared with external 1.05V SVR
L9401: STUFF	L9401: NO STUFF
R9413: NO STUFF	R9413: STUFF
R9402: STUFF	R9402: NO STUFF
R9403: NO STUFF	R9403: STUFF

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply. When sharing, make sure the 1.05V_LAN is controlled by the SLP_LAN signal.

Note : LAN Chip must be changed to I218LM (71.00218.E03)



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File: **LAN INTEL WGI218LM**

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<Core Design>



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Title

LAN SW

Size
A4

Document Number

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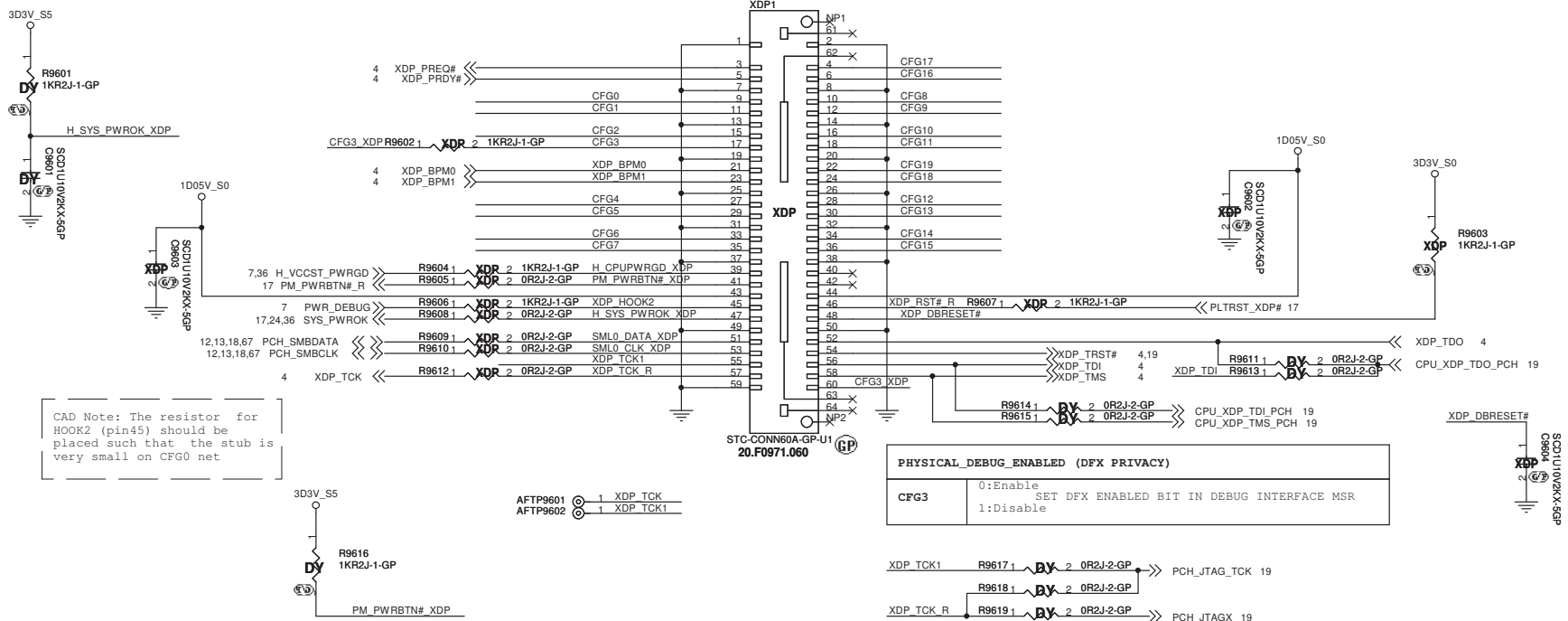
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SSID = CPU_XDP

CPU_XDP

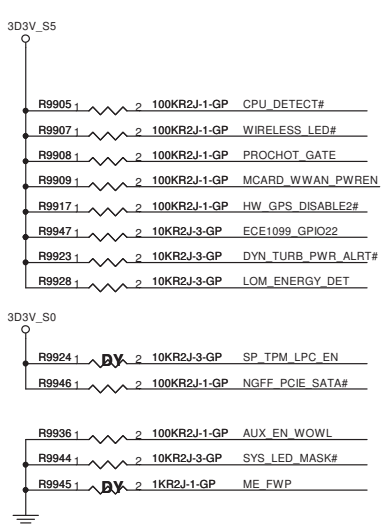
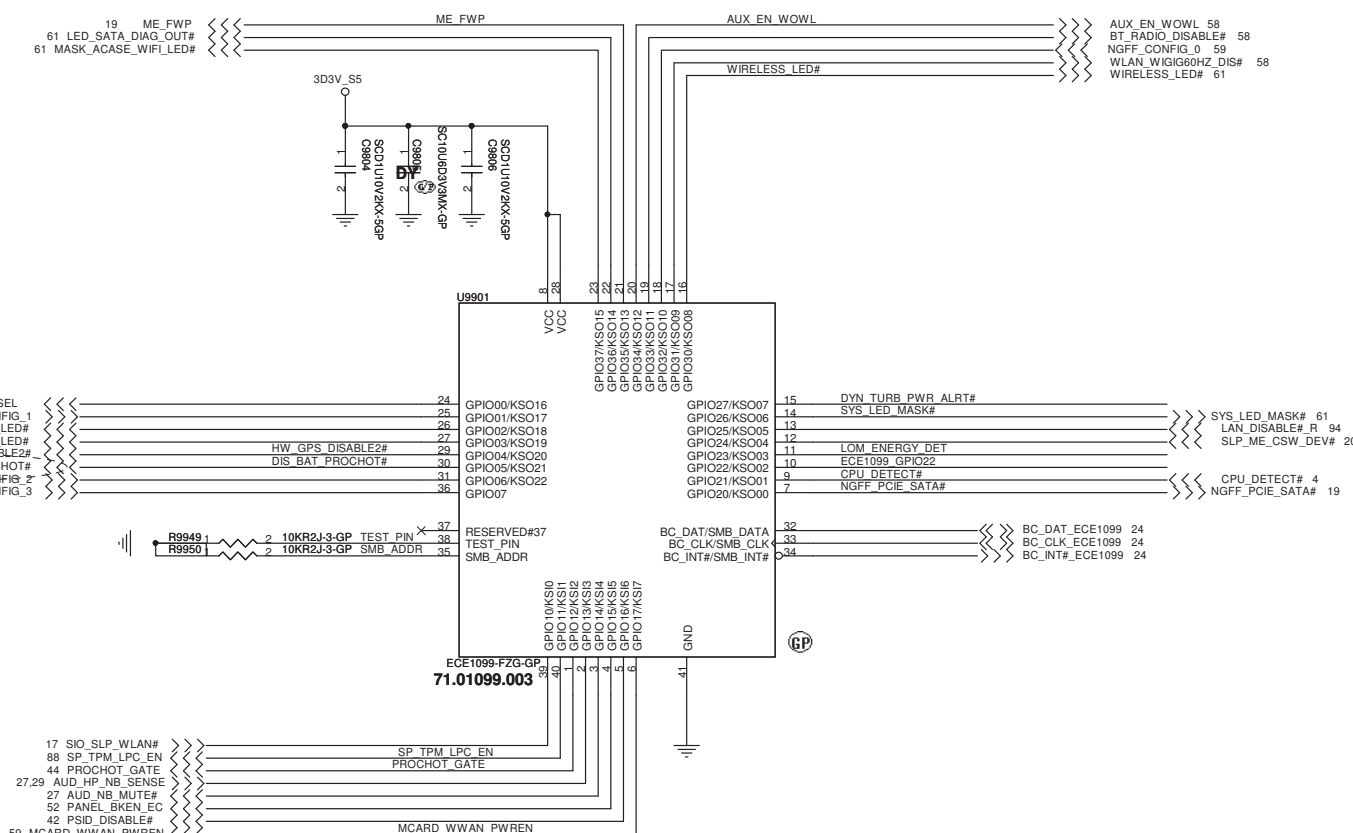


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Title			
USB2.0 HUB			
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SSID = SIO



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File: **SIO - ECE1099**

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